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     FILE 'WPIX, JAPIO' ENTERED AT 11:26:51 ON 13 SEP 2002
L1       872042 S IC OR ICS OR ((INTEGRATED OR LOGIC)(W)(CIRCUIT)) OR (MICRO)(W
L2       332013 S LASER OR IRASER OR QUANTUM(W)GENERATOR
L3       559624 S TAN OR TA OR TIN OR TI OR W OR WN OR TASIN OR TISIN OR TA()N
L4       184776 S ((TANTALUM OR TITANIUM OR TUNGSTEN)(N)(NITRIDE)) OR TANTALUM
L5       149923 S POLYIMIDE OR POLYAMIDE OR POLYARLYENE OR POLYARYLENE OR (POLY
L6        21455 S L1 AND L2
L7         1088 S L6 AND L3
L8          296 S L6 AND L4
L9         1311 S L7 OR L8
L10          32 S L9 AND L5
L11          25 S L9 AND (CONDUCTIV?)(N)(LAYER? OR FILM OR COAT####)
L12          23 S L11 NOT L10
L13         241 S L6 AND L5
L14          11 S L13 AND (CONDUCTIV?)(N)(LAYER? OR FILM OR COAT####)
L15       11539 S S05-A03A2/MC OR (A61N-005 OR S05-A03A)/IC
L16         180 S L1 AND L15
L17           0 S L16 NOT L16
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L10 ANSWER 1 OF 32 WPIX (C) 2002 THOMSON DERWENT
AN 2002-314871 [35] WPIX
DNN N2002-246483 DNC C2002-091514
TI Fabrication of surface mountable **chip** inductor for electric appliances, involves forming spiral coil pattern on surface of cylindrical body, and transforming body into square-shaped body.
DC A18 A23 A85 L03 P42 V02 X12
IN AHN, B; AHN, B J
PA (CERA-N) CERATECH CORP; (SERA-N) SERATECH CO LTD
CYC 4
PI US 2002013994 A1 20020207 (200235)* 13p
CN 1336673 A 20020220 (200235)
JP 2002118026 A 20020419 (200243) 8p
KR 2002010782 A 20020206 (200255)
ADT US 2002013994 A1 US 2001-915703 20010726; CN 1336673 A CN 2001-123810 20010730; JP 2002118026 A JP 2001-231073 20010731; KR 2002010782 A KR 2000-44252 20000731
PRAI KR 2001-25833 20010511; KR 2000-44252 20000731; KR 2000-66089 20001108
AB US2002013994 A UPAB: 20020603
NOVELTY - Surface mountable **chip** inductor is fabricated by forming a cylindrical body (10) by mixing ferrite or ceramic powder with thermoplastic organic binder, forming a coil pattern on a surface of the body, and transforming the body into a square-shaped body by inserting the body with the coil pattern into a square-shaped mold and applying pressure to the body at certain temperature.
USE - For fabricating a surface mountable **chip** inductor used for electric appliances, e.g. electronic home appliances and electronic industrial equipment.
ADVANTAGE - By forming a coil pattern on the cylindrical body and transforming the cylindrical body into a square shaped body, an electric characteristic lowering problem is prevented. The invention is simple, is advantageous to mass production, and lowers cost. The **chip** inductor can be easily mounted using conventional **chip** mounter.
DESCRIPTION OF DRAWING(S) - The drawing shows a cylindrical body having a spiral metal coil pattern on a surface.
cylindrical body 10
thread-shaped flexible material 30
Dwg.3A/8

L10 ANSWER 2 OF 32 WPIX (C) 2002 THOMSON DERWENT
AN 2002-253492 [30] WPIX
DNN N2002-195601 DNC C2002-075836
TI **Laser** accessible fuse formation in **integrated circuit** comprises etching **laser** access opening in two steps using transient etch stop layers to limit access opening depth after first step and finishing opening in second step.
DC L03 U11
IN CHEN, Y; TZENG, W; WANG, K
PA (VANG-N) VANGUARD INT SEMICONDUCTOR CORP
CYC 1
PI US 6294474 B1 20010925 (200230)* 11p
ADT US 6294474 B1 US 1999-425906 19991025
PRAI US 1999-425906 19991025
AB US 6294474 B UPAB: 20020513
NOVELTY - A **laser** accessible fuse is formed in an

integrated circuit by etching a **laser** access opening in two steps using a transient etch stop layers to limit the depth of the access opening after the first step and finishing the opening in the second step.

DETAILED DESCRIPTION - Formation of a **laser** accessible fuse in an **integrated circuit** involves:

(a) providing a silicon **wafer** (10) having **integrated circuit** devices and a first insulative layer;

(b) patterning a fusible material layer on the first insulative layer to form a fuse (18) with a rupture zone;

(c) depositing a silicon oxide layer on the **wafer**;

(d) patterning a polysilicon layer over the silicon oxide layer to form a first plate overlying the rupture zone;

(e) depositing a second insulative layer over the **wafer**;

(f) forming conductive contacts to the fuse on through openings in the second insulative layer and the silicon oxide layer, by which the rupture zone is connected between, and in electrical series with, at least two of the conductive contacts;

(g) patterning a first metal layer (34) having a super-adjacent first antireflective coating (ARC), on the second insulative layer to form a first inter-connective wiring level to the devices and the fuse, and a second plate, concentric with the first plate overlying the rupture zone;

(h) depositing a third insulative layer over the **wafer**;

(i) patterning the third insulative layer and penetrating first ARC, to form via openings and an access opening (46) which exposes the second plate;

(j) patterning a second metal layer (50) having a super-adjacent second ARC, on the third insulative layer to form bonding pads connected to the inter-connective wiring through vias in the third insulative layer, while simultaneously removing both the second metal layer and the second plate in the access opening;

(k) depositing a passivation layer (68) on the **wafer**;

(l) patterning the passivation layer and the ARC by anisotropically etching, with a first etchant gas mixture and a first silicon oxide-to-polysilicon selectivity, to expose the bonding pads and a region within the window opening, penetrating the third and second insulative layers, and stopping on the first plate; and

(m) after step (l), without breaking vacuum and with a second gas mixture and a second silicon oxide-to-polysilicon selectivity, etching through the first plate and partially into the second insulative layer, leaving a final thickness of the second insulative layer over the rupture zone.

USE - Forming a **laser** accessible fuse in an **integrated circuit**.

ADVANTAGE - The process provides improved control of dielectric thickness over the fuse. It also fits conveniently within the framework of an existing process and does not introduce any additional steps.

DESCRIPTION OF DRAWING(S) - The figure is a cross section of a portion of a Dynamic Random Access Memory **integrated circuit**.

Wafer 10
Fuse 18
First metal layer 34
Access opening 46
Second metal layer 50
Passivation layer 68
Dwg.1F/1

L10 ANSWER 3 OF 32 WPIX (C) 2002 THOMSON DERWENT
AN 2002-054429 [07] WPIX
DNN N2002-040079 DNC C2002-015432
TI Coaxial connector for interconnecting high frequency electronic devices, comprises gold-plated conductive wire core surrounded by dielectric layer, which is also surrounded by **tin**-plated layer of conductive material.
DC A85 V04
IN BUDMAN, M; INTERRANTE, M J; KNICKERBOCKER, J U
PA (IBMC) INT BUSINESS MACHINES CORP
CYC 1
PI US 6302732 B1 20011016 (200207)* 6p
ADT US 6302732 B1 US 1999-460888 19991214
PRAI US 1999-460888 19991214
AB US 6302732 B UPAB: 20020130
NOVELTY - A coaxial connector comprises a conductive wire core (1) surrounded by a thin layer of gold for connection to a signal pad. The gold layer is surrounded by a dielectric layer (7), and the surface of the dielectric layer comprises a conductive shielding layer (9) coated with a thin layer of **tin** (11) for connection to an adjacent ground pad.

DETAILED DESCRIPTION - A coaxial connector comprises a conductive wire core having a diameter of 20-30 mu m surrounded by a thin layer of gold for connection to a signal pad. The gold layer is surrounded by a dielectric layer. The surface of the dielectric layer comprises a conductive shielding layer coated with a thin layer of **tin** for connection to an adjacent ground pad. The gold-plated conductive wire core extends beyond the dielectric layer by a distance not greater than the required to connect to the signal pad and accommodates the high frequency electronic device signal to ground pad spacing.

An INDEPENDENT CLAIM is also included for a method of coaxially interconnecting high frequency electronic devices comprising removing a portion of **tin**-plated conductive shielding layer contiguously surrounding gold-plated conductive wire, and wire bonding the gold-plated conductive wire to one of the signal pads, and soldering the **tin** -plated conductive shielding layer to an adjacent one of the ground pads.

USE - For interconnecting high frequency electronic devices, e.g. silicon germanide semiconductor **chip**.

ADVANTAGE - The invention has minimal unshielded wire, has reduced noise coupling between high electronic devices, and is effective for making multiple high density connections. It can be minimally striped of shielding material by **laser** ablation to the pitch of the input/output pads. Effective bonding connection to electronic devices is simply achieved by wire bonding.

DESCRIPTION OF DRAWING(S) - The figure shows an end view of a coaxial wire conductor.

Conductive wire core 1
Dielectric layer 7
Conductive shielding layer 9
Tin layer 11
Dwg.1/2

L10 ANSWER 4 OF 32 WPIX (C) 2002 THOMSON DERWENT
AN 2001-308035 [32] WPIX
CR 2000-013482 [01]
DNN N2001-220449 DNC C2001-095124
TI Providing two-stage solder bump on **wafer** surface by applying

underfill material to substrate, applying bump(s) to the assembly, applying flux to the surface to cover the exposed portions of the caps.

DC A85 L03 M23 U11
IN BLUMEL, D; GILLEO, K B
PA (ALPH-N) ALPHA METALS INC; (FRYM) FRYS METALS INC
CYC 94
PI WO 2001020676 A1 20010322 (200132)* EN 25p
RW: AT BE CH CY DE DK EA ES FI FR GB GH GM GR IE IT KE LS LU MC MW MZ NL OA PT SD SE SL SZ TZ UG ZW
W: AE AG AL AM AT AU AZ BA BB BG BR BY BZ CA CH CN CR CU CZ DE DK DM DZ EE ES FI GB GD GE GH GM HR HU ID IL IN IS JP KE KG KP KR KZ LC LK LR LS LT LU LV MA MD MG MK MN MW MX MZ NO NZ PL PT RO RU SD SE SG SI SK SL TJ TM TR TT TZ UA UG UZ VN YU ZA ZW
US 6228681 B1 20010508 (200133)
AU 2000074847 A 20010417 (200140)
ADT WO 2001020676 A1 WO 2000-US25152 20000914; US 6228681 B1 CIP of US 1999-266166 19990310, US 1999-395558 19990914; AU 2000074847 A AU 2000-74847 20000914
FDT AU 2000074847 A Based on WO 200120676
PRAI US 1999-395558 19990914; US 1999-266166 19990310
AB WO 200120676 A UPAB: 20020528

NOVELTY - Two-stage solder bump is provided on a **wafer** surface by applying an underfill material to a substrate having solderable contact site(s). A bump(s) of a first composition is applied to the assembly, which occupies each aperture in the underfill, and extends above the underfill material. A flux is applied to the surface to cover at least the exposed portions of the caps.

DETAILED DESCRIPTION - Providing a two-stage solder bump on a **wafer** (12) surface, comprises applying an underfill material (14) to a substrate (24) having solderable contact site(s), in a manner which covers the substrate surface and the solderable contact site(s). The underfill material is treated to form an aperture(s) extending entirely through the underfill material, and is located so that it exposes only the solderable contact site. A bump(s) (18) of a first composition is applied to the assembly in a manner so that it occupies each aperture in the underfill, contacts the exposed solderable contact site, and extends above the underfill material. A cap (20) formed of a second composition is applied to the bump(s). A flux (22) is applied to the surface to cover at least the exposed portions of the caps.

USE - For providing two-stage solder bump on a **wafer** surface.

ADVANTAGE - The method is a simple and inexpensive process, which simultaneously provides flux and underfill as part of the flip **chip**.

DESCRIPTION OF DRAWING(S) - The figure shows a schematic representation of the masked substrate.

wafer 12
underfill material 14
bump 18
cap 20
flux 22
substrate 24
Dwg.7/8

L10 ANSWER 5 OF 32 WPIX (C) 2002 THOMSON DERWENT
AN 2001-183010 [18] WPIX
DNN N2001-130598 DNC C2001-054671

TI Singulation of electronic circuits involves aligning **laser** beam with feature or fiducial of laminated material joining circuits, and training beam along material until cut has been made.
DC A21 A26 A85 L03 P55 U11 V04 X24
IN BOYLE, A; CONLON, P; MAHON, J; OWEN, M
PA (XSIL-N) XSIL TECHNOLOGY LTD
CYC 95
PI WO 2001010177 A1 20010208 (200118)* EN 45p
RW: AT BE CH CY DE DK EA ES FI FR GB GH GM GR IE IT KE LS LU MC MW MZ NL OA PT SD SE SL SZ TZ UG ZW
W: AE AG AL AM AT AU AZ BA BB BG BR BY BZ CA CH CN CR CU CZ DE DK DM DZ EE ES FI GB GD GE GH GM HR HU ID IL IN IS JP KE KG KP KR KZ LC LK LR LS LT LU LV MA MD MG MK MN MW MX MZ NO NZ PL PT RO RU SD SE SG SI SK SL TJ TM TR TT TZ UA UG US UZ VN YU ZA ZW
AU 2000061782 A 20010219 (200129)
IE 81922 B 20010919 (200172)
EP 1201108 A1 20020502 (200236) EN
R: AL AT BE CH CY DE DK ES FI FR GB GR IE IT LI LT LU LV MC MK NL PT RO SE SI
ADT WO 2001010177 A1 WO 2000-IE95 20000803; AU 2000061782 A AU 2000-61782 20000803; IE 81922 B IE 2000-618 20000803; EP 1201108 A1 EP 2000-948225 20000803, WO 2000-IE95 20000803
FDT AU 2000061782 A Based on WO 200110177; EP 1201108 A1 Based on WO 200110177
PRAI IE 1999-664 19990803
AB WO 200110177 A UPAB: 20010402
NOVELTY - An electronic circuit is singulated by generating a **laser** beam having a wavelength of less than 400 nm, a minimum energy density of 100 J/cm2 or a minimum peak power density of 1 GW/cm2, aligning the beam with a feature or fiducial of laminated material joining the circuits, and training the beam along the material until cut has been made.

DETAILED DESCRIPTION - An INDEPENDENT CLAIM is also included for a circuit singulation system comprising mechanism for supporting a set of electronic circuits interconnected by material, a **laser** beam source (33), and a beam positioning mechanism.

USE - For cutting circuit boards, **integrated circuit** packages or flex circuits, cutting thin layers, e.g. liquid crystal sheets or electrochromic dielectric thin films useful in displays.

ADVANTAGE - The method achieves a maximum cut rate at repetition frequency. It provides a higher yield by reducing the extent of deposited debris and by reducing handling requirements. It uses **laser** creating excellent quality cuts which generate only vapor debris, use no consumables, do not cause any **chips** or micro-cracks in the cut edge, and do not incur cost like a diamond saw for, e.g. **wafer** saw.

DESCRIPTION OF DRAWING(S) - The drawing shows a control of a **laser** beam for cutting.

Laser beam source 33
Mirrors 37, 38
Camera 39
Focusing lens 40
Dwg.2/9

L10 ANSWER 6 OF 32 WPIX (C) 2002 THOMSON DERWENT
AN 2001-168046 [17] WPIX
DNN N2001-121187 DNC C2001-050065

TI Fabrication of multilayer **microelectronic** interconnect structure used in high density interconnects for high performance **microelectronic** device **chips** uses a low dielectric constant material, e.g. air as the intralevel dielectric.

DC A85 L03 U11 U14

IN BUCHWALTER, L P; CALLEGARI, A C; COHEN, S A; GRAHAM, T O; HUMMEL, J P; JAHNES, C V; PURUSHOTHAMAN, S; SAENGER, K L; SHAW, J M

PA (IBMC) INT BUSINESS MACHINES CORP

CYC 1

PI US 6184121 B1 20010206 (200117)* 18p

ADT US 6184121 B1 Provisional US 1997-52174P 19970710, US 1998-112919 19980709

PRAI US 1997-52174P 19970710; US 1998-112919 19980709

AB US 6184121 B UPAB: 20010328

NOVELTY - A multilayer **microelectronic** interconnect structure is fabricated by using a low dielectric constant material, e.g. air as the intralevel dielectric which reduces intralevel capacitance.

DETAILED DESCRIPTION - A multilayer **microelectronic** interconnect structure is fabricated by (i) applying a double layer thickness of a thermally stable and easily processable dielectric material (20, 30) having a top layer and a lower layer on a semiconductor **wafer** (10); (ii) patterning and etching trenches for wiring tracks on the top layer and vias in the lower layer; (iii) depositing a thin electrically conductive barrier/adhesion layer (60) in the trenches and vias and overfilling the trenches and vias with a thick conductive wiring layer metal; (iv) planarizing the wiring layer metal by etching or polishing to achieve a coplanar inlaid structure of conductors and vias embedded as metal features in the dielectric material; (v) repeating steps (i-iv) until a requisite number of wiring levels in the interconnect structure are fabricated; (vi) removing the dielectric metal from all areas of the **wafer** not directly covered by the conductors by means of an etching process while leaving the dielectric material intact under the metal feature; (vii) optionally applying a thin conformal passivation layer (100) to cap and protect the exposed metal features; (viii) annealing the etched structure at an elevated temperature in a reducing atmosphere to mitigate any plasma process induced damage; (ix) laminating a thin taut insulating cover layer (120) to the top surface of the passivated metal features; (x) optionally depositing a thin insulating environmental barrier layer (130) on top of the cover layer; (xi) etching terminal vias in the optional barrier layer, insulating cover layer, and the thin conformal passivation layer to provide access for terminal pad contacts; and (xii) depositing and patterning terminal metal pads at the via locations to complete the interconnect structure.

USE - For use in high density interconnects for high performance **microelectronic** device **chips**, e.g. for logic, memory, communication, and microcontroller applications.

ADVANTAGE - The i structure possesses a very low capacitance and fast propagation speeds.

DESCRIPTION OF DRAWING(S) - The figure shows a schematic sketch of the interconnect structure after terminal vias have been etched and terminal pads are deposited to complete the fabrication of the structure.

Semiconductor **wafer** 10

Double layer of dielectric material 20, 30

Thin electrically conductive barrier/adhesion layer 60

Thin conformal passivation layer 100

Thin taut insulating cover layer 120

Thin insulating environmental barrier layer 130

Dwg.4D/7

L10 ANSWER 7 OF 32 WPIX (C) 2002 THOMSON DERWENT
AN 2001-141734 [15] WPIX
DNN N2001-103536 DNC C2001-042227
TI **Polyimide** film forming method for semiconductor device manufacture, involves solidifying film on peripheral edge portion of **wafer**, after removing film formed on circumferential portion of **wafer**.
DC A85 L03 P42 U11
IN SAKAMOTO, Y; YAEGASHI, H
PA (TKEL) TOKYO ELECTRON LTD; (SAKA-I) SAKAMOTO Y; (YAEG-I) YAEGASHI H
CYC 2
PI JP 2000323471 A 20001124 (200115)* 14p
US 6284044 B1 20010904 (200154)
US 2001041229 A1 20011115 (200172)
ADT JP 2000323471 A JP 2000-43138 20000221; US 6284044 B1 US 2000-520158 20000307; US 2001041229 A1 Div ex US 2000-520158 20000307, US 2001-905134 20010716
FDT US 2001041229 A1 Div ex US 6284044
PRAI JP 1999-60399 19990308
AB JP2000323471 A UPAB: 20010919
NOVELTY - The **polyimide** liquid is supplied on **wafer** (W) to form **polyimide** film (P) of predetermined thickness on its surface. Then, the film formed on circumferential portion of **wafer** is removed by supplying clean liquid and irradiating the surface using **laser** beam. After which, film on the edge of peripheral portion of **wafer** is solidified.
DETAILED DESCRIPTION - An INDEPENDENT CLAIM is also included for **polyimide** film forming apparatus.
USE - For semiconductor device manufacture.
ADVANTAGE - Prevents drying of process liquid in center portion of **wafer**, and flow of liquid into the circumference part of **wafer**, even when **wafer** is moved.
DESCRIPTION OF DRAWING(S) - The figure shows the sketchy explanatory diagram of film forming apparatus.
Wafer W
Polyimide film P
Dwg.4/21

L10 ANSWER 8 OF 32 WPIX (C) 2002 THOMSON DERWENT
AN 2001-137243 [14] WPIX
DNN N2001-099933 DNC C2001-040177
TI Formation of **laser** accessible fuse for memory arrays by forming fuse with rupture zone, patterning metal layer to form conductive wiring connected to conductive contacts, plate over rupture zone, and wiring pad, patterning passivation layer.
DC L03 U11 U13 U14
IN LIN, H; TZENG, W; YANG, C
PA (VANG-N) VANGUARD INT SEMICONDUCTOR CORP
CYC 1
PI US 6180503 B1 20010130 (200114)* 17p
ADT US 6180503 B1 US 1999-354852 19990729
PRAI US 1999-354852 19990729
AB US 6180503 B UPAB: 20010312
NOVELTY - A **laser** accessible fuse is formed by forming a fuse with a rupture zone; patterning a metal layer to form conductive wiring connected to at least two conductive contacts, a plate over the rupture

zone, and a wiring pad; patterning a passivation layer by anisotropically etching the passivation layer and an anti-reflective coating over a bonding pad, forming a **laser** access window.

DETAILED DESCRIPTION - A **laser** accessible fuse is formed by:

(a) depositing a layer of fusible material on a first insulative layer on a silicon **wafer** (70);

(b) patterning the layer of fusible material to form a fuse (78) with a rupture zone (78A);

(c) depositing a second insulative layer over the **wafer**;

(d) forming conductive contacts to the fuse through openings in the second insulative layer, where the rupture zone is connected between, and in electrical series with, at least two of the conductive contacts;

(e) depositing a first metal layer (94) on the second insulative layer;

(f) patterning the first metal layer to form conductive wiring (96) connected to each of at least two conductive contacts, a plate (86) over the rupture zone, and a wiring pad;

(g) depositing a third insulative layer over the **wafer**;

(h) patterning the third insulative layer to form a via opening to the wiring pad, and a window opening over the rupture zone;

(i) depositing a second metal layer (108) on the **wafer**;

(j) depositing an anti-reflective coating (92) on the second metal layer;

(k) patterning a bonding pad in the second metal layer over the via opening and removing the anti-reflective coating, the second metal layer, and the first metal layer in the window opening;

(l) depositing a passivation layer over the **wafer**; and

(m) patterning the passivation layer by anisotropically etching the passivation layer and the anti-reflective coating over the bonding pad while simultaneously etching a region within the window opening, penetrating the second insulative layer to a final second insulative layer thickness over the rupture zone, forming a **laser** access window.

USE - For forming a **laser** accessible fuse for memory arrays useful in computer memory **chips**, e.g., dynamic random access memory (DRAM).

ADVANTAGE - The invention (a) allows for a simultaneous etching of the passivation layer and bonding pad openings; (b) retards fuse access opening formation during via formation using the transient etch stop layers; (c) improves the uniformity of insulative layers over fuse links while at the same time over-etches vias and passivation layer access openings to thoroughly remove anti reflection coating layers; and (d) uses a single photolithographic mask for patterning a passivation layer to form access to bonding pads and **laser** access openings.

DESCRIPTION OF DRAWING(S) - The figure shows a cross-section of a DRAM with a fuse access window formed.

Wafer 70
Fuse 78
Rupture zone 78A
Plate 86
Anti-reflective coating 92
First metal layer 94
Conductive wiring 96
Second metal layer 108
Silicon oxide 118
Silicon nitride 119
Polyimide 120

Passivation layer 122
Dwg.2E/2

L10 ANSWER 9 OF 32 WPIX (C) 2002 THOMSON DERWENT
AN 2000-497852 [44] WPIX
DNN N2000-368925 DNC C2000-149307
TI Method of tape auto bonding of ball grid array package **chips** comprises reducing the size of **chip** packaging with ball grid array.
DC A85 L03 U11
IN TSAI, W
PA (COMP-N) COMPEQ MFG CO LTD
CYC 1
PI TW 377478 A 19991221 (200044)* 19p
ADT TW 377478 A TW 1997-111657 19970814
PRAI TW 1997-111657 19970814
AB TW 377478 A UPAB: 20000918
NOVELTY - Method of tape auto bonding of ball grid array package **chips**. Due to the expensive cost of base material for improved TAB-BGA packaging and inaccurate positioning by implantation of solder balls, it is difficult to reduce the size of solder joint. Furthermore, this kind of circuit packaging must go through wire bonding process, making the packaged volume even larger. The process under this invention includes: (1) Using **polyimide** material for the substrate, with one side coupled with copper plate, which is etched to form contact holes; (2) Electroplating its surface with copper/**tin**, and electrolyzing the holes to form protuberances for solder joints; (3) Etching away the surface coating of copper, and removing **tin** layer; (4) Drilling holes with **laser**; and (5) Covering up sputtering mask. A miniaturized solder joint is thus formed externally for **chip** coupling, requiring only a single solder joint. It can therefore reduce the size of **chip** packaging.
Dwg.1/3

L10 ANSWER 10 OF 32 WPIX (C) 2002 THOMSON DERWENT
AN 2000-399064 [34] WPIX
DNN N2000-298936 DNC C2000-120392
TI Semiconductor device fuse for use in semiconductor memory comprises fuse material and dielectric material on a portion of fuse material, with thickness of dielectric material so as to minimize reflectance.
DC A26 A85 L03 U11 U13 U14
IN CASTAGNETTI, R; GIUST, G K; LIU, Y; RAMESH, S
PA (LSIL-N) LSI LOGIC CORP
CYC 1
PI US 6061264 A 20000509 (200034)* 16p
ADT US 6061264 A US 1998-118602 19980717
PRAI US 1998-118602 19980717
AB US 6061264 A UPAB: 20000718
NOVELTY - A semiconductor device fuse comprises a fuse material and a dielectric material disposed on a portion of fuse material. The thickness of dielectric material is such that the reflectance of incident **laser** light from the dielectric material is less than that from the fuse material.
DETAILED DESCRIPTION - INDEPENDENT CLAIMS are also included for the following: (i) Semiconductor memory comprising plurality of rows and columns, and a semiconductor device fuse. (ii) Semiconductor memory device comprising memory array, plurality of metal layers overlaying memory array

with at least one of the metal layers provides electrical connection to the array, and a semiconductor device fuse in metal layers.

USE - The semiconductor device fuse is used for semiconductor memory which is used in semiconductor memory device. The semiconductor memory device is used as **integrated circuit** (claimed).

ADVANTAGE - A semiconductor device fuse has self alignment fuse structure which allows photolithographic control and effective size reduction of the **laser** spot irradiating the fuse material and surrounding structure in semiconductor fuse technology. This permits reduced fuse pitch, increasing density and the efficiency of use of **chip** area, and results in reduced thermal exposure, which causes less damage to **chip**. In addition, **laser** alignment is less critical and therefore less time-consuming, which increases throughput in fabrication. The fuse exploits the characteristics of dielectric material that its reflectance changes with its thickness due to optical interference effect. The anti-reflective dielectric layer is of optimized thickness so that incident **laser** light used to blow the fuse is transmitted through the dielectric to the fuse material with increased absorption into the fuse material than the conventional where blanket dielectric capping layer was used. The fuse material below dielectric absorbs more energy. The **wafer**'s thermal exposure is reduced due to increased reflectance outside of the patterned area. The fuse material receives much more fluence than the surrounding area within the diameter of beam of incident **laser** energy. The **laser** alignment step is made less critical even if the center of the **laser** beam is slightly misaligned to patterned dielectric area, the **laser** fluence can be increased without harming the region outside fuse region due to the fuse region absorbing more energy from the **laser**.

Dwg.0/6

L10 ANSWER 11 OF 32 WPIX (C) 2002 THOMSON DERWENT
AN 2000-365916 [31] WPIX
DNN N2000-273819 DNC C2000-110600
TI Thin, chemically metallizable, adhesion promoting layer for insulating materials, especially polymer substrates for **microelectronics**, comprises a metal with an oxygen concentration gradient.
DC L03 V04
IN KICKELHAIN, J; VITT, B
PA (LPKF-N) LPKF LASER & ELECTRONICS AG
CYC 20
PI WO 2000027175 A1 20000511 (200031)* DE 13p
RW: AT BE CH CY DE DK ES FI FR GB GR IE IT LU MC NL PT SE
W: JP US
DE 19850592 C1 20001012 (200051)
ADT WO 2000027175 A1 WO 1999-DE3465 19991029; DE 19850592 C1 DE 1998-19850592 19981103
PRAI DE 1998-19850592 19981103
AB WO 200027175 A UPAB: 20000630
NOVELTY - A thin, chemically metallizable, adhesion promoting layer for insulating materials, comprises a metal with an oxygen concentration gradient.

DETAILED DESCRIPTION - A thin, chemically metallizable, metal oxide-based adhesion promoting layer for insulating materials, for producing adherent conductor structures by **laser** irradiation, is 20-200 nm thick and has a region, adjacent the insulating material, which has an oxygen concentration decreasing constantly from a maximum value to

zero in the direction away from the insulating material and which contains one or more of copper, chromium, nickel and **titanium** or a mixture of copper with **tin** or zinc.

An INDEPENDENT CLAIM is also included for production of the above adhesion promoting layer by cathodic sputtering or plasma- or **laser**-assisted chemical vapor deposition (CVD).

USE - As an adhesion promoting layer for production of **laser** structured conductor lines on insulating substrates (especially of **polyimide, polyamide,** acrylonitrile butadiene styrene (ABS), polyethylene (PET), polypropylene and polycarbonate) for **microelectronics**.

ADVANTAGE - The gradient composition layer provides extremely good adhesion to the underlying (usually flexible) insulating material and to a chemical metallization (e.g. an adhesive strength of greater than 15 N/cm to the metallization), without mechanical stress and low conductivity problems caused by a constant oxygen content.

Dwg.0/0

L10 ANSWER 12 OF 32 WPIX (C) 2002 THOMSON DERWENT
AN 2000-291981 [25] WPIX
DNN N2000-218908 DNC C2000-088146
TI Collet arrangement for handling **integrated circuit** structures has a main body with a portion connectable to a vacuum source and with interior chamber, and depending collets with contact area.
DC A85 L03 P54 U11
IN FREUND, J M; PRZYBYLEK, G J; ROMERO, D M
PA (LUCE) LUCENT TECHNOLOGIES INC
CYC 1
PI US 6036196 A 20000314 (200025)* 6p
ADT US 6036196 A US 1998-178899 19981026
PRAI US 1998-178899 19981026
AB US 6036196 A UPAB: 20000524

NOVELTY - A collet arrangement (110) for handling **integrated circuit** structures has a main body (114) with a portion connectable to a vacuum source and having an interior chamber in communication with vacuum source when connected; and depending collets in communication with chamber, each positioned in a spaced relationship over the **integrated circuit** and with lower contact end having a contact area.

USE - For handling **integrated circuit** structures during manufacture.

ADVANTAGE - The collets have hollow interiors, providing opening which is 8 mils in diameter. The collet's contact area is smaller than the smallest dimension of the **laser** bar, thus reducing damage from contact of collet. Circuit structures of various shapes could be handled efficiently by arranging the spaced collets near the periphery of the structure. No adjustment is needed in the collet arrangement, when used to handle individual **laser chips** previously cleaved from the bar.

DESCRIPTION OF DRAWING(S) - The figure shows a side view of a collet arrangement configured to handle **laser** bars, the collet shown to pick up a **laser** bar.

Collet arrangement 110
Main body 114
Collets 116, 118
Dwg.3/3

L10 ANSWER 13 OF 32 WPIX (C) 2002 THOMSON DERWENT
AN 2000-052267 [04] WPIX
CR 2000-401299 [33]; 2001-417175 [41]
DNN N2000-040769 DNC C2000-013436
TI Contact lead manufacturing method for probe cards.
DC A85 L03 P84 Q68 S01 U11 V04
IN FRAME, J W; JONES, M R; KHOURY, T A
PA (ADVA-N) ADVANTEST KK; (ADVA-N) ADVANTEST CORP
CYC 5
PI US 5989994 A 19991123 (200004)* 15p
JP 2000162241 A 20000616 (200036) 12p
SG 75186 A1 20000919 (200055)
KR 2000035748 A 20000626 (200111)
TW 440897 A 20010616 (200203)
ADT US 5989994 A US 1998-222176 19981229; JP 2000162241 A JP 1999-337754 19991129; SG 75186 A1 SG 1999-5775 19991119; KR 2000035748 A KR 1999-53374 19991129; TW 440897 A TW 1999-120847 19991130
PRAI US 1998-222176 19981229; US 1998-201299 19981130
AB US 5989994 A UPAB: 20020114
NOVELTY - The method involves aligning a photomask having an image of leads over a photoresist layer formed on an electric conductive layer formed on a sacrificial layer of a silicon substrate, exposing the photoresist to radiation, developing the image, forming electric conductive leads (30) by metal deposition, separating the leads from the substrate.

DETAILED DESCRIPTION - An adhesion promoter layer made of chromium or **titanium** may be formed between the sacrificial layer formed on the surface of the silicon substrate and the conductive layer. The sacrificial layer is made of silicon dioxide. The conductive layer is made of copper or nickel. The photoresist material used is M-Cresol-formaldehyde, poly methyl methacrylate, or photosensitive **polyimide**. The photoresist layer is directly exposed by an electron beam, X-ray or **laser** light to define the image of the contact leads or the photoresist layer is exposed to X-rays through the photomask. The image developed has openings on the surface of the photoresist layer. The contact leads are formed in the openings by depositing a metal selected from copper, nickel, aluminum, rhodium, palladium or **tungsten** by electroplating. The electric conductive material used for the conductive layer is different from the electric conductive material for the contact leads. After metal deposition, the photoresist layer is stripped and the contact leads are separated from the silicon substrate by a primary etching process and from the conductive layer by a secondary etching process. The method involves a photolithography process comprising the steps of photoresist coating, masking, exposure, photoresist stripping and conductive material deposition. The leads produced are in a horizontal direction on the silicon substrate, and the surfaces of the leads are polarized. Instead of the etching process, alternatively, an adhesive tape is applied on the contact leads to remove the leads from the substrate and the conductive layer. An INDEPENDENT CLAIM is also included for a method of producing a contact mechanism having contact leads each of which exhibits a spring force for establishing electrical contact with a contact target. The contact mechanism such as a probe card is produced by positioning the adhesive tape having the contact leads, and removing the leads and orienting the leads in a predetermined direction. The leads are placed on a predetermined position on a bonding location (32) of a substrate (20) of the contact mechanism and are bonded to the bonding location.

USE - For contact leads to be mounted on a probe card used for testing high density and high speed electrical devices such as LSI and VLSI circuits, semiconductor **wafers**, burn-in of semiconductor **wafers**, testing and burn-in of packaged semiconductor devices, printed circuit boards etc, and for forming leads of **IC chips** or **IC** packages.

ADVANTAGE - The method enables to mount a large number of contact leads on a probe card in a vertical direction in order to electrically contact the targets such as contact pads on a printed circuit board. The method is able to produce a large number of contact leads in a horizontal direction on the silicon substrate by using the relatively simple technique utilizing a single photolithography step and hence the method is highly efficient and cost effective. The contact leads have high mechanical strength and reliability. The contact leads are of higher reliability because of the simplified production process. The contact leads exhibit spring force for establishing electrical contact with a contact target as they are mounted vertically.

DESCRIPTION OF DRAWING(S) - The figure shows the schematic view of a pick and place mechanism for picking and placing the contact leads on substrate such as probe card.

Substrate 20

Electric conductive leads 30

Bonding location 32

Dwg.5B/7

L10 ANSWER 14 OF 32 WPIX (C) 2002 THOMSON DERWENT
AN 1999-419186 [35] WPIX
CR 2002-507624 [54]
DNN N1999-312876 DNC C1999-123293
TI Micro-electromechanically tunable surface emitting **laser** and Fabry-Perot filter.
DC A85 L03 P81 U12 V07 V08
IN AZIMI, M; TAYEBATI, P; VAKHSHOORI, D; WANG, P
PA (CORE-N) CORETEK INC; (AZIM-I) AZIMI M; (TAYE-I) TAYEBATI P; (VAKH-I) VAKHSHOORI D; (WANG-I) WANG P
CYC 84
PI WO 9934484 A2 19990708 (199935)* EN 74p
RW: AT BE CH CY DE DK EA ES FI FR GB GH GM GR IE IT KE LS LU MC MW NL OA PT SD SE SZ UG ZW
W: AL AM AT AU AZ BA BB BG BR BY CA CH CN CU CZ DE DK EE ES FI GB GD GE GH GM HR HU ID IL IN IS JP KE KG KP KR KZ LC LK LR LS LT LU LV MD MG MK MN MW MX NO NZ PL PT RO RU SD SE SG SI SK SL TJ TM TR TT UA UG UZ VN YU ZW
AU 9920174 A 19990719 (199951)
EP 1053574 A2 20001122 (200061) EN
R: DE FR GB IT
CN 1285034 A 20010221 (200131)
JP 2002500446 W 20020108 (200206) 57p
US 2002031155 A1 20020314 (200222)
US 6438149 B1 20020820 (200257)
ADT WO 9934484 A2 WO 1998-US27681 19981228; AU 9920174 A AU 1999-20174 19981228; EP 1053574 A2 EP 1998-964965 19981228, WO 1998-US27681 19981228; CN 1285034 A CN 1998-813831 19981228; JP 2002500446 W WO 1998-US27681 19981228, JP 2000-527004 19981228; US 2002031155 A1 US 1998-105399 19980626; US 6438149 B1 US 1998-105399 19980626
FDT AU 9920174 A Based on WO 9934484; EP 1053574 A2 Based on WO 9934484; JP 2002500446 W Based on WO 9934484

PRAI US 1998-105399 19980626; US 1997-68931P 19971229
AB WO 9934484 A UPAB: 20020906
NOVELTY - Micro-electromechanically tunable surface emitting **laser** and Fabry-Perot filter have precise lateral and vertical dimension control and use preselected strain introduced into the quantum well structure to optimize gain performance.
DETAILED DESCRIPTION - A preselected amount and type of strain is introduced into the quantum wells of a pre-grown crystalline semiconductor by depositing at least one thin film onto the upper surface of the member comprising the quantum wells, the thin film having an amount and type of strain opposite to that required in the member.
INDEPENDENT CLAIMS are included for the following: (a) a micromechanically tunable vertical cavity surface emitting **laser** (VCSEL) and Fabry-Perot filter having precise lateral and vertical dimension control. Controlled strain in the quantum well structure of the devices is used to provide optimized gain performance; (b) methods for fabrication of the VCSEL and filter.
USE - As wavelength tunable surface emitting semiconductor **lasers** and filters used in opto-electronics.
ADVANTAGE - The devices have precise dimensional control and have controlled strain in the quantum well regions so that gain properties are optimized.
DESCRIPTION OF DRAWING(S) - The drawing shows a micro-electromechanical tunable filter of the invention with a confocal cavity. Dwg.1/7

L10 ANSWER 15 OF 32 WPIX (C) 2002 THOMSON DERWENT
AN 1999-328028 [28] WPIX
DNN N1999-245979 DNC C1999-097298
TI Packaging **integrated circuit** - comprises etching copper of **polyimide** film, forming holes and electroplating.
DC A85 L03 U11
IN CAI, W
PA (HUAT-N) HUATONG COMPUTER CO LTD
CYC 1
PI CN 1209649 A 19990303 (199928)*
ADT CN 1209649 A CN 1997-117534 19970827
PRAI CN 1997-117534 19970827
AB CN 1209649 A UPAB: 19990723
Roll automatic welded ball grid array **integrated circuit** packaging comprises: covering **polyimide** film, with pressure joined thin copper layer of both sides, with first dry film; etching lower layer of thin copper to form several notches; **laser** drilling to form several holes corresponding to the notches on the **polyimide** film; covering that with secondary dry film, and electroplating its upper surface to form copper plated and **tin** plated layers; removing lower layer of thin copper, and electrolytic electroplating the holes to form outwards projected contacts; and etching top layer of thin copper, stripping plated **tin**, **laser** drilling and covering with sputtered masks to form sputtered salient points used for welding **chip**, so that it can make external contacts much fine, and can reduce package area.

L10 ANSWER 16 OF 32 WPIX (C) 2002 THOMSON DERWENT
AN 1999-189060 [16] WPIX
DNN N1999-138228 DNC C1999-055497
TI Methods for packaging tab-BGA **integrated circuits** - a

method for packaging a TAB-BGA **integrated circuit**, comprises providing a **polyimide** with a pre-laminated thin copper layer on each of two sides thereof; etc..

DC A85 L03 U11
IN TSAY, W
PA (COMP-N) COMPEQ MFG CO LTD
CYC 1
PI TW 345711 A 19981121 (199916)*
ADT TW 345711 A TW 1997-111740 19970815
PRAI TW 1997-111740 19970815
AB TW 345711 A UPAB: 19990424
A method for packaging a TAB-BGA **integrated circuit**, comprising steps of: providing a **polyimide** with a pre-laminated thin copper layer on each of two sides thereof as a substrate; etching the lower layer thin copper of the **polyimide** using a first dry film as the mask, thereby forming a plurality of **chips**; carrying out a **laser** drilling on the **polyimide** portion of the substrate using the lower layer thin copper as the mask, thereby forming a pattern of holes; carrying out electro-coppering and electrotinning on the upper surface of the substrate using a second dry film as the mask; etching to remove the lower layer thin copper using a third dry film as the mask; electroplating the holes on the **polyimide** film using a fourth dry film to protect the upper layer of the substrate, thereby forming electroplated contacts filling up the holes and slightly protruding outwards therefrom; selectively etching the exposed thin copper and electroplated **tin**, thereby separating adjacent electroplated coppers from each other, the exposed thin copper being between the electroplated coppers; performing a **laser** drilling operation at the center of the substrate and at locations needing a through hole, thereby separately forming a **chip** mounting hole at the center of the substrate and peripheral **laser** through holes; covering a mask and exposing the near end edges of the electroplated copper at the center of the substrate; sputtering a metal thereby forming sputtering protruding spots corresponding to the exposed portion of the electroplated copper; and removing the mask and mounting a **chip** corresponding to the sputtering protruding spots.

L10 ANSWER 17 OF 32 WPIX (C) 2002 THOMSON DERWENT
AN 1999-146577 [13] WPIX
DNN N1999-106896 DNC C1999-043109
TI Liquid coating apparatus for semiconductor **wafer**, glass substrate of photomask, LCD, optical disk substrate - has controller which adjusts execution timing of supply initiation and stoppage instructions of processing program based on timing signal generated corresponding to light reflected from substrate.
DC A89 G06 L03 P42 P84 T03 U11 U14 W04
PA (DNIS) DAINIPPON SCREEN SEIZO KK
CYC 1
PI JP 11010054 A 19990119 (199913)* 10p
ADT JP 11010054 A JP 1997-162726 19970619
PRAI JP 1997-162726 19970619
AB JP 11010054 A UPAB: 19990331
NOVELTY - A light receiver (29) receives the reflected light from a substrate (**W**) irradiated by a light transmitter (27). A **laser** receiver (33) receives the output of light receiver and generates an electrical signal depending on the supply state of liquid to the substrate. An integrating circuit (35) removes the noise in the

electrical signal and outputs a shaping signal to a differential circuit (37) which shapes the received signal as a timing signal. A controller (20) adjusts the execution timing of the supply initiation and stoppage instructions of a processing program based on the timing signal. The liquid supply is performed based on the execution of instructions.

USE - For coating photoresist liquid, **polyimide** resin on semiconductor **wafer**, glass substrate for photomasks, LCD, optical disk substrate.

ADVANTAGE - Prevents malfunctioning resulting from the splash of liquid. Coating is correctly adjustable by adjusting the execution timing of instructions.

DESCRIPTION OF DRAWING(S) - The drawing shows a block diagram of the coating apparatus. (W) Substrate ; (5) Liquid supply nozzle ; (20) Controller ; (27) Light transmitter ; (29) Light receiver ; (33) **Laser** receiver ; (35) Integration circuit ; (37) Differentiating circuit.

Dwg.1/7

L10 ANSWER 18 OF 32 WPIX (C) 2002 THOMSON DERWENT
AN 1996-289447 [30] WPIX
DNN N1996-242928 DNC C1996-092605
TI **Laser** surface treatment of electronic modules support band - using rectilinear shaped **laser** spot with power controlled as function of sweep speed to remove protective surface layer.
DC A35 A85 P76 T04 V04
IN GAUMET, M; GOUILLER, M; THEVENOT, B; VERE, D
PA (SOLA-N) SOLAIC SA
CYC 27
PI FR 2727780 A1 19960607 (199630)* 10p
WO 9726109 A1 19970724 (199735)# FR 14p
RW: AT BE CH DE DK ES FR GB GR IE IT LU MC NL PT SE
W: AU BR BY CA CN JP KR MX RU SG UA
AU 9645433 A 19970811 (199747)#
BR 9603594 A 19990615 (199929)#
ADT FR 2727780 A1 FR 1994-14463 19941201; WO 9726109 A1 WO 1996-FR62 19960115; AU 9645433 A AU 1996-45433 19960115, WO 1996-FR62 19960115; BR 9603594 A BR 1996-3594 19960115, WO 1996-FR62 19960115
FDT AU 9645433 A Based on WO 9726109; BR 9603594 A Based on WO 9726109
PRAI FR 1994-14463 19941201; WO 1996-FR62 19960115; AU 1996-45433 19960115; BR 1996-3594 19960115
AB FR 2727780 A UPAB: 19960731
Surface treatment of a plastic band (1) having on one face a support piece (2) of predetermined width, on which are fixed modules (3) for electronic cards, has been developed. The modules have **microcircuits** (6) embedded in a protective resin (7) that projects above the support surface.

The method consists of: irradiating the support piece (2) with a **laser** beam (10) able to form a rectilinear spot (12) extending over the whole width of the support piece; moving the band w.r.t the beam to permit the spot to longitudinally sweep the support; measuring the speed of displacement of the band w.r.t. the beam; adjusting the beam emission as a function of ing the speed so it continuously removes a superficial layer of plastic and protective resin from the support and module.

Also claimed is the appts. to implement the process.

USE - Used in prodn. of electronic cards partic. with

polyamide band surfaces.
ADVANTAGE - Eliminates use of aggressive mechanical or chemical methods that could damage the electronic modules.
Dwg.1/1

L10 ANSWER 19 OF 32 WPIX (C) 2002 THOMSON DERWENT
AN 1996-202166 [21] WPIX
CR 1996-170951 [17]; 1996-202165 [21]; 1997-238280 [22]; 1997-424129 [39]; 1998-505540 [43]; 1999-213997 [18]; 2000-557535 [43]; 2001-464392 [23]; 2001-557263 [23]
DNN N1996-169615
TI Fully integrated miniaturised liquid sample handling and analysis device for liquid phase analysis of small or macromolecular solutes - uses **laser** ablation of microchannel into surface of planar substrate with channel covered to form sample processing compartment.
DC S03
IN BEK, F; KALTENBACH, P; MITTELSTADT, L S; SWEDBERG, S A; WITT, K E
PA (HEWP) HEWLETT-PACKARD CO
CYC 7
PI EP 708331 A1 19960424 (199621)* EN 38p
R: CH DE GB LI SE
US 5571410 A 19961105 (199650) 35p
JP 08334505 A 19961217 (199709) 30p
US 36350 E 19991026 (199952)
ADT EP 708331 A1 EP 1995-116515 19951019; US 5571410 A CIP of US 1994-326111 19941019, US 1995-486024 19950607; JP 08334505 A JP 1996-166933 19960606; US 36350 E CIP of US 1994-326111 19941019, US 1995-486024 19950607, US 1998-127556 19980730
FDT US 5571410 A CIP of US 5500071; US 36350 E CIP of US 5500071, Reissue of US 5571410
PRAI US 1995-486024 19950607; US 1994-326111 19941019; US 1998-127556 19980730
AB EP 708331 A UPAB: 20011031
The system (200) includes a miniaturised planar column (2) with microstructures fabricated by **laser** ablation in a variety of novel support substrates (4). The substrate generally comprises two planar opposing surfaces (6,8) and is selected from material other than silicon which is UV absorbing and is accordingly **laser**-ablatable.
The device has a column structure ablated on a **chip**, which is machinable form of plastic **polyimide**. The substrate has a microchannel (10) **laser** ablated on one surface. A cover plate (12) is arranged over the surface and the microchannel to form an elongated sample processing compartment (14).
ADVANTAGE - Provides miniaturized column device **laser** -ablated in planar substrate.
Dwg.1/18

L10 ANSWER 20 OF 32 WPIX (C) 2002 THOMSON DERWENT
AN 1995-274267 [36] WPIX
DNC C1995-124409
TI Prodn. of thin-film hybrid **integrated circuit** arrangement - includes evapn. of copper target by pulse **laser** radiation of determined energy density, and deposition on **polyimide** substrate which is at room temp..
DC L03
IN BYKOVSKII, YU A; KORPUKHIN, A S; KOZLENKOV, V P
PA (MOEP) MOSC ENG PHYS INST

CYC 1
PI SU 1748623 A1 19950220 (199536)* 3p
ADT SU 1748623 A1 SU 1990-4811985 19900409
PRAI SU 1990-4811985 19900409
AB SU 1748623 A UPAB: 19950918
Prodn. of thin-film hybrid **integrated circuit** arrangement includes evapn. of copper target in vacuum by pulse **laser** radiation with energy flow density on the target surface of 109-1010 W/cm2., depositing the vapour onto a **polyimide** substrate which is at room temp., and forming the pattern arrangement by photolithography.

In the evapn. of a copper target by pulse **laser** radiation with energy flux density 109-1010 W/cm2., a plasma cluster comprising ions with energy of 10-1000 eV (around 30% of all particles) and neutral atoms with energy of 1-100 eV is formed Bombardment of the surface of a **polyimide** substrate by the particles removes contaminant molecules of residual gases and low mol. wt. fractions from the substrate. The action of particles with energy at and above 10 eV leads to partial destruction and modification of the outer layers of the **polyimide** and the production of a large number of broken bonds, chemically active radicals and oxygen-contg. gps.. At the time of condensation of the copper vapour onto the **polyimide** substrate, the particles penetrate the surface layers, forming a copper-enriched **polyimide** layer.

USE - Mfr. of non-housed **integrated circuits**.

ADVANTAGE - Improved quality of lay-out can be achieved since the adhesion of copper to the substrate is increased and changes in the linear dimensions of the substrate are reduced.
Dwg.0/1

L10 ANSWER 21 OF 32 WPIX (C) 2002 THOMSON DERWENT
AN 1995-131976 [18] WPIX
DNN N1995-103808 DNC C1995-060877
TI Temp. resistant relief structures for use in printed circuits etc. - includes coating a substrate with soluble hydroxy **polyimide** or soluble poly phenyl quinoxaline, irradiating with a pulsed UV **laser**, and developing..
DC A26 A89 G06 L03 P84 U11 V04
IN AHNE, H; HAMMERSCHMIDT, A; ROTH, W; ZAPF, L
PA (SIEI) SIEMENS AG
CYC 1
PI DE 4332876 A1 19950330 (199518)* 8p
ADT DE 4332876 A1 DE 1993-4332876 19930927
PRAI DE 1993-4332876 19930927
AB DE 4332876 A UPAB: 19950518
The prodn. of highly heat-resistant relief structures comprises coating a substrate with a layer of a soluble hydroxypolyimide of formula (I) or a soluble polyphenylquinoxaline of formula (II), irradiating through a mask with a pulsed UV **laser** at a wavelength of less than 300 nm and a power density of more than 105 W/cm2, and developing the image; R, R1, R*, R1* = aromatic or heterocyclic gps.; n1, n2 = 1-100; n = 2-1000; R2, R3 = H, alkyl, haloalkyl, aryl, halo, OH, CN, -CC-R4 or -SiMe (with R4 = H, alkyl, aryl or SiMe3); Ar1 = benzene-1,2,4,6-tetrayl, naphthalene-2,3,6,7-tetrayl or =Ar-(X1)s-Ar= (with Ar = o-phenyleneyl; X1 = -(CH2)t-, -(CF2)t-, -O-, -CO-, -S-, -SO-, -SO2- or -C(CF3)2-, -C(R5)2-, -Si(R5)3- or -NR5- [with t = 1-10 and R5 = H or alkyl]; s = 0 or 1); Ar2 = phenylene, naphthylene or -phenylene-(X2)s-phenylene- (with s = 0 or 1,

and X2 = as for X1).

USE - Used for the prodn. of dielectric interlayers in multilayer circuits on **chips**, planarising layers for levelling **wafer** topography, dielectrics for multilayer printed circuits boards for wiring **integrated circuits**, and passivating layers on **chips** or micro-circuitry.

ADVANTAGE - Enables the prodn. of high-grade, temp.-resistant relief structures with high resolution, without extra tampering at 400 deg.C as in prior-art processes (i.e. no loss of thickness due to tempering, resulting in a better aspect ratio, a simple process requiring only short drying at up to 200 deg.C, homogeneous layers with no tempering peaks, very pure layers with no initiator, improved storage stability due to the absence of unsatd. gps., reduced stress due to temp. differences). Dwg.0/0

L10 ANSWER 22 OF 32 WPIX (C) 2002 THOMSON DERWENT
AN 1993-367855 [46] WPIX
DNN N1993-284011 DNC C1993-163240
TI Metal deposition on a substrate for **microcircuits** and **chips** - by selective seeding of the metal by excimer **laser** radiation through the metal ion contg. soln..
DC A35 L03 M13 P42 U11 X25
IN BRAREN, B E; OSULLIVAN, E J M; SCHROTT, A G
PA (IBMC) IBM CORP; (IBMC) INT BUSINESS MACHINES CORP
CYC 2
PI US 5260108 A 19931109 (199346)* 6p
JP 06081153 A 19940322 (199416) 6p
ADT US 5260108 A US 1992-849273 19920310; JP 06081153 A JP 1993-5668 19930118
PRAI US 1992-849273 19920310
AB US 5260108 A UPAB: 19940103
A deposit of metal is formed on a substrate selected from **polyimide**, silicon dioxide, **tantalum** oxide and polyethylene terephthalate, the substrate having a surface. The process comprises: 1) contacting surface (12) of substrate (10) with a soln. (14) contg. ions of the metal to be deposited; 2) providing a source of **laser** light (22) having a wavelength such that the **laser** light is capable of being absorbed by substrate (10); 3) exposing surface (12) to **laser** light (18) through soln. (14) at a wavelength which renders the **laser** light absorbable by the substrate while simultaneously maintaining a fluence and a power density effective to release electrons from the substrate; ions of the metal are thus reduced and thereby deposit the metal onto the surface without causing thermal activation of soln. (14) or substrate (10).

USE/ADVANTAGE - In the mfr. of e.g. **microcircuits** and **chips**. Advantage is taken of the **laser** in a way which permits the operator to avoid imprecision in finely detailed operation and procedures which result from the use and/or generation of heat. Dwg.1/1

L10 ANSWER 23 OF 32 WPIX (C) 2002 THOMSON DERWENT
AN 1993-086850 [11] WPIX
CR 1994-161161 [20]
DNN N1993-066453 DNC C1993-038261
TI Compsn. having lower thermal coefft. of expansion - comprises fluorinated carbon **polyimide** composites used in mfr. of electronic components and circuits, etc..
DC A26 A85 L03 U11 V04 X12

IN AFZALI-ARDAKANI, A; BRAREN, B E; DAIJAVAD, S; HODGSON, R T; MOLIS, S E; VIEHBECK, A
PA (IBMC) INT BUSINESS MACHINES CORP; (IBMC) IBM CORP
CYC 4
PI EP 531764 A1 19930317 (199311)* EN 11p
R: DE FR GB
JP 07073151 B2 19950802 (199535) 14p
EP 531764 B1 19971022 (199747) EN 10p
R: DE FR GB
DE 69222824 E 19971127 (199802)
ADT EP 531764 A1 EP 1992-114138 19920819; JP 07073151 B2 JP 1992-241572 19920910; EP 531764 B1 EP 1992-114138 19920819; DE 69222824 E DE 1992-622824 19920819, EP 1992-114138 19920819
FDT JP 07073151 B2 Based on JP 06061597; DE 69222824 E Based on EP 531764
PRAI US 1991-759377 19910913; US 1991-759380 19910913; US 1992-929313 19920813
AB EP 531764 A UPAB: 19940715
A compsn. of matter comprises 2-50 wt.% of a fluorinated particulate carbon material dispersed in a **polyimide** polymer material.

Also claimed are: (i) a process for effecting a change in the physical properties of a **polyimide** material partic. dielectric constant and reduced coefft. of thermal expansion comprising forming a compsn. of matter and heating the composite material at elevated temps.; and (ii) the formation of a **polyimide** composite with at least one surface conductive region in the polymer composite material contg. a fluorinated C material comprising irradiating the **polyimide** composite material with a pulsed UV **laser**.

The compsn. further comprises a coupling agent in an amt. suffucient to enhance the dispersability of the fluorinated carbon material in the **polyimide** precursor material. The **polyimide** material is imidised **polyimide**, and is formed from polyamic acids or ester of polyamic acids. Pref. the **polyimide** material is based on PMDA-ODA, BDA-PDA or BTDA-APB. The **polyimide** material comprises a solvent soluble **polyimide**, a solvent soluble polyetherimide or a polyisoimide. The fluorinated carbon material contains up to 75 atomic wt.% of F. The coupling agent is an organo Si cpd. or an organo **Ti** cpd.

USE/ADVANTAGE - Useful in the mfr. of electronic components and electronic circuits e.g. **microelectronic** circuits, printed circuits and circuit boards. Composites can be converted into high or low dielectric constant proide
Dwg.0/1
Dwg.0/1

L10 ANSWER 24 OF 32 WPIX (C) 2002 THOMSON DERWENT
AN 1993-029662 [04] WPIX
DNN N1993-022726 DNC C1993-013195
TI Grindstone for precision machining semiconductor **wafer**, **laser** mirror etc. - comprises resin-bonded abrasive grains of non-stoichiometric cpd. including metal oxide, oxy carbide, oxynitride and/or solid soln..
DC A81 L02 P61
PA (TTUN) TOSHIBA TUNGALLOY KK
CYC 1
PI JP 04354676 A 19921209 (199304)* 7p
JP 3014062 B2 20000228 (200015) 8p
ADT JP 04354676 A JP 1991-155584 19910530; JP 3014062 B2 JP 1991-155584

19910530
FDT JP 3014062 B2 Previous Publ. JP 04354676
PRAI JP 1991-155584 19910530
AB JP 04354676 A UPAB: 19930924
A resin-bonded grinding stone comprises 30 vol. % or more of abrasive grains of a non-stoichiometric cpd. composed of metal oxide(s), metal oxycarbide(s), metal oxynitride(s), and their solid solns..
Pref. the abrasive grains are composed of oxides, oxycarbides, and/or oxynitrides of **Ti**, Cr, or Fe, or their solid solns.. The abrasive grains are 1.0 micron or less in average dia.. The griding stone comprises 15-49 vol. % of a resin and 30-80 vol. % of the abrasive grains; pref., the resin is phenol, epoxy, **polyimide**, polystyrene, and/or polyethylene resins.
USE/ADVANTAGE - For mirror finishing semiconductor **wafers**, magnetic head substrates, reflection mirrors for **lasers**, optical parts, precision machine parts, electronic parts, etc..
0/0

L10 ANSWER 25 OF 32 WPIX (C) 2002 THOMSON DERWENT
AN 1992-183968 [22] WPIX
DNN N1992-138813 DNC C1992-084291
TI Repairing electrical wiring in printed circuit boards - using **laser** ablation to dress the site and repairing with **polyamide** insulator with devices in place.
DC A85 L03 M23 P55 U11 U14 V04
IN HANDFORD, E F; HARVILCHUCK, J M; INTERRANTE, M J; JACKSON, R A; MASTER, R N; RAY, S K; SABLINSKI, W E; WASSICK, T A
PA (IBMC) INT BUSINESS MACHINES CORP
CYC 2
PI WO 9208337 A1 19920514 (199222)* EN 45p
US 5153408 A 19921006 (199243) 11p
JP 05507391 W 19931021 (199347) 45p
US 5543584 A 19960806 (199637) 11p
ADT WO 9208337 A1 WO 1991-US541 19910125; US 5153408 A US 1990-607969 19901031; JP 05507391 W JP 1991-516583 19910125, WO 1991-US541 19910125; US 5543584 A Div ex US 1990-607969 19901031, US 1992-843684 19920228
FDT JP 05507391 W Based on WO 9208337; US 5543584 A Div ex US 5153408
PRAI US 1990-607969 19901031; US 1992-843684 19920228
AB WO 9208337 A UPAB: 19931006
Restoring an electrically conducting path across a defect in an electrical line comprises (a) ablating an area around the defect; (b) placing a segment of an electrically conducting material over a portion of the electrical line; and (c) securing the segment to the line, thereby forming an electrically conductive path.
USE/ADVANTAGE - Used to repair electrical conductors, partic. those having open circuit faults, in high-density PCBs. The process allows repairs to be performed in the presence of active components, e.g., **chips**, and passive components, e.g., capacitors, pins, discrete wires, etc.. Multiple repairs can be accomplished in one step. (2B,3,4/6)
2B,3,4/6

L10 ANSWER 26 OF 32 WPIX (C) 2002 THOMSON DERWENT
AN 1992-096244 [12] WPIX
DNN N1992-072045 DNC C1992-044644
TI **Laser** ablation damascene process for planarising metallised substrate - simultaneously fills substrate depressions with metal andablate metal from surface areas.

DC A85 L03 R46 U11
IN ANDRESHAK, J C; BASEMAN, R J; BA
PA (IBMC) INT BUSINESS MACHINES CORP; (IBMC) IBM CORP
CYC 5
PI US 5093279 A 19920303 (199212)* 9p
EP 497180 A2 19920805 (199232) EN 10p
R: DE FR GB
EP 497180 A3 19930428 (199401)
JP 06168943 A 19940614 (199428) 11p
ADT US 5093279 A US 1991-653209 19910201; EP 497180 A2 EP 1992-100866 19920120; EP 497180 A3 EP 1992-100866 19920120; JP 06168943 A JP 1991-325274 19911113
PRAI US 1991-653209 19910201
AB US 5093279 A UPAB: 19931006
Laser ablation damascenee process for planarising a surface comprises: depositing a metal layer to at least partially fill depressions in the substrate and deposit on the surrounding surface area; and applying **laser** pulse(s) of a fluence such that metal melts and fills completely the depressions while being ablated from the surrounding surface area. The depressions are pref. vias and trenches forming metallisation in an **IC** interconnect structure.
Substrate is an organic insulator, esp. **polyimide**. The metallisation is Cu. An intermediate adhesion-promoting layer, pref. **Ta**, **Ti** or Cr, is included. The thicknesses of the substrate, intermediate layer and Cu layer are respectively 2.0, 0.2 and 3.2 micron. The **laser** pulse is a 15ns, 532 nm 2.5 J/sq.cm. visible pulse produced by frequency doubling a 1.04 micron IR **laser** output. Other suitable **lasers** are UV, visible and IR **lasers**. Debris formed may be simultaneously removed.
ADVANTAGE - Depressions are filled and surface metal ablated in a single step.
3/6

L10 ANSWER 27 OF 32 WPIX (C) 2002 THOMSON DERWENT
AN 1991-261772 [36] WPIX
DNN N1991-199698 DNC C1991-113617
TI Electronic circuit for microwave frequency - with conductive regions obtd. by irradiating polymer layer with ion beam.
DC A26 A85 L03 U11 U14 X12
IN BROUSSOUX, D; BUREAU, J M
PA (CSFC) THOMSON CSF
CYC 5
PI EP 445040 A 19910904 (199136)*
R: DE GB IT
FR 2659171 A 19910906 (199146)
JP 04217317 A 19920807 (199238) 5p
ADT EP 445040 A EP 1991-400570 19910301; FR 2659171 A FR 1990-2653 19900302; JP 04217317 A JP 1991-59522 19910301
PRAI FR 1990-2653 19900302
AB EP 445040 A UPAB: 19930928
Fabricating an electric circuit comprises depositing a layer of polymer (2) and irradiating this with an ion beam to render it more conductive and to define at least one element (3) of the electric circuit.
The polymer is pref. a thermally stable polymer, esp. a **polyimide** or a polyphenyl quinoxaline.
USE/ADVANTAGE - Process allows treatment either of polymer layers on a substrate, or of self-supporting polymer films. Unlike previous

processes for circuit prodn. consisting, e.g., of screen printing or conductive inks contg. Au or Pd-Ag alloys, or vacuum metallisation with Ni or Cr, the present procedure does not require the prodn. of new masks for each application and can be used for prodn. of 3-dimensional circuits as opposed to the only 2-dimensional circuits which could be produced previously. Process is esp. useful for prodn. of hyperfrequency **integrated circuits**, esp. Microwave **Integrated Circuits** (MIC) and Monolithic Microwave **Integrated Circuits** (MMIC).

In an example, a film (2) ca. 2 micrometres thick of a thermally stable polymer was formed on a dielectric substrate (1), e.g., of Al, silica, PTFE, Ga arsenate, **Ti** oxide, etc.. Onto the polymer layer are formed propagation lines for electromagnetic waves and active elements forming part of an electric circuit. Subsequently one or more conductive zones (3) are created by irradiation with an ion beam or a **laser** beam. Beam can be spatially guided and modulated **w** .r.t. power and rate.of scanning by a suitable control system.
2/9

L10 ANSWER 28 OF 32 WPIX (C) 2002 THOMSON DERWENT
AN 1991-107717 [15] WPIX
DNN N1991-153707 DNC C1991-046602
TI Focused ultrasound for microscopic patterning of polymers - comprising submerging focusing transducer in water and directing focused beam at **polyimide**.
DC A35 A85 U11 X25
PA (ANON) ANONYMOUS
CYC 1
PI RD 323099 A 19910310 (199115)*
PRAI RD 1991-323099 19910220
AB RD 323099 A UPAB: 19930928
Patterning polymers with micron sized features using ultrasound rather than conventional patterning that uses photoresist or **laser** ablation is claimed. At present our feature size is in the 100 micron range but we fully expect that 1-10 microns can be achieved by going to higher acoustic frequencies than we have so far used. With a 10 MHz sound wave in water, localised swelling or the formation or ridges and/or holes results when the ultrasound is focussed onto **polyimide** (Kapton). The smallest feature size at 10 MHz is between 50-100 microns, close to the diffraction limited spot size of the acoustic beam.

Patterning is achieved by submerging the spherically shaped front surface focussing transducer (Precision Acoustic Devices, Fremont, CA) in water and directing the focussed beam at the polymer, also submerged in water. Experimentally, for a 50-micron-thick sheet of Kapton (Dupont Reg. TM) we have observed patterns in the form of raised ridges, - 20-30 microns high, 100 microns wide for an effective incident acoustic power level of only 1000 **W**/cm2 with the substrate scanned at 250 microns/s. Similar patterns have been fabricated on polymethylmethacrylate (PMMA). With an acoustic microscope in the gigahertz range, the pattern will be smaller in proportion to the reduced wavelength, i.e., on the order of 1 micron.

USE - This type of patterning in Kapton and other polymers is ideally suited for **microelectronic** application

L10 ANSWER 29 OF 32 WPIX (C) 2002 THOMSON DERWENT
AN 1988-246984 [35] WPIX
DNN N1988-238897 DNC C1988-139072

TI **Laser** butt welded cans from steel sheet - using blanks with resin coating on inner surface adjoining mating edges to prevent adhesion of melted metal particles etc.
DC A18 A28 A82 M23 P55 Q32 X24
PA (TOXD) TOX DUEBEL WERK; (TOXO) TOYO SEIKAN KAISHA LTD
CYC 3
PI JP 63180389 A 19880725 (198835)* 67p
GB 2202779 A 19881005 (198840)
US 4805795 A 19890221 (198910) 16p
US 4840304 A 19890620 (198931) 17p
GB 2202779 B 19900530 (199022)
ADT JP 63180389 A JP 1987-10961 19870120; GB 2202779 A GB 1987-30221 19871229; US 4805795 A US 1987-140603 19871228; US 4840304 A US 1988-239662 19880902
PRAI JP 1986-310194 19861227; JP 1987-3022 19870109; JP 1987-10959 19870120; JP 1987-10960 19870120; JP 1987-10961 19870120

L10 ANSWER 30 OF 32 WPIX (C) 2002 THOMSON DERWENT
AN 1987-336428 [48] WPIX
DNN N1987-251900 DNC C1987-143560
TI Refractory metal or metal silicide interconnects or resistors - deposited by **laser** induced direct writing pyrolysis on **polyimide** film substrates.
DC A85 L03 P42 P73 U11
IN BLACK, J G; EHRLICH, D J
PA (MASI) MASSACHUSETTS INST TECHNOLOGY
CYC 15
PI EP 247783 A 19871202 (198748)* EN 25p
R: AT BE CH DE ES FR GB GR IT LI LU NL SE
JP 63024640 A 19880202 (198810)
US 4756927 A 19880712 (198830) 10p
US 4957775 A 19900918 (199040)
ADT EP 247783 A EP 1987-304466 19870520; JP 63024640 A JP 1987-134814 19870529; US 4756927 A US 1986-868615 19860529; US 4957775 A US 1988-165927 19880309
PRAI US 1986-868615 19860529
AB EP 247783 A UPAB: 19930922
Refractory metal or metal silicide patterns are formed on a semiconductor substrate by **laser**-induced direct writing pyrolysis using a flowing gas mixt. of two reactants and an inert gas (pref. Ar), the reactants comprising **W**, Mo or **Ti** fluorides or chlorides and a gaseous Si- or Ge-contg. cpd. The **laser** irradiation power, typically 40 mW, is sufficient to initiate, localise,and guide the reaction between the two reactants; the Si or Ge cpd. provides a catalyst to sustain the reaction and permit formation of the desired pattern on the substrate. Pref. the substrate has an exposed **polyimide** film surface upon which a pattern with good adhesion is formed. Pref., the reactants are WF6 and SiH4 and the bulk resistivity of the deposited layer varies with, and can be controlled by, the WF6:SiH4 ratio.

USE/ADVANTAGE - At high WF6:SiH4 ratios a low resistivity metallic pattern of **W** is formed and the process is then used to provide interconnections between circuit elements in the mfr. of semiconductor **integrated circuits** or for the repair of defective circuit interconnects. At low WF6:SiH4 ratios, high resistance patterns of predetermined resistance are formed and the process is used for direct deposition of resistors on semiconductor substrates. Use of **polyimide** film as an inert, stress-relieving material on the

substrate surface ensures good adhesion of the refractory metal and protects the substrate from chemical attack.
1D/5

L10 ANSWER 31 OF 32 JAPIO COPYRIGHT 2002 JPO
AN 2000-323471 JAPIO
TI FILM FORMING METHOD AND DEVICE
IN SAKAMOTO YASUHIRO; YAEGASHI HIDETAMI
PA TOKYO ELECTRON LTD
PI JP 2000323471 A 20001124 Heisei
AI JP 2000-43138 (JP2000043138 Heisei) 20000221
PRAI JP 1999-60399 19990308
SO PATENT ABSTRACTS OF JAPAN (CD-ROM), Unexamined Applications, Vol. 2000
AB PROBLEM TO BE SOLVED: To prevent a processing solution from flowing to the periphery of a **wafer** even if the **wafer** is moved before the processing solution applied on the **wafer** is not dried out yet.
SOLUTION: A **polyimide** film is formed on a **wafer** **W** through a film forming device 15 through a manner where **polyimide** liquid is fed on the **wafer W** while the **wafer** is spun by a spin chuck 56, where an irradiatiating device 81 which radiates the periphery of the **wafer W** with a **laser** beam is provided in the film forming device 15. A **polyimide** film is formed on the **wafer W**, and after the **wafer W** is subjected to a side rinsing treatment, the periphery of the **wafer W** is irradiated with a **laser** beam to solidify the film formed on the periphery of the **wafer W**. The solidified **polyimide** film serves as a dam to prevent **polyimide** solution from flowing out of the periphery of the **wafer W**.
COPYRIGHT: (C)2000,JPO

L10 ANSWER 32 OF 32 JAPIO COPYRIGHT 2002 JPO
AN 1989-057695 JAPIO
TI HYBRID **INTEGRATED CIRCUIT**
IN FUKUDA NOBUO
PA NEC CORP
PI JP 01057695 A 19890303 Heisei
AI JP 1987-214243 (JP62214243 Showa) 19870827
PRAI JP 1987-214243 19870827
SO PATENT ABSTRACTS OF JAPAN (CD-ROM), Unexamined Applications, Vol. 1989
AB PURPOSE: To form a thin film resistance circuit having the cross part of circuits oh one sheet of a substrate and to obtain a hybrid **integrated circuit** mounted with various components by a method wherein a first thin film conductor film is formed on the insulating substrate, an interlayer insulating film having apertures is formed thereon, a second thin film conductor film having apertures are formed thereon and the like.
CONSTITUTION: A first thin film conductor film 3 formed on an insulating ceramic substrate 1, an interlayer insulating film 5, which is formed on the film 3 and has apertures 6 to reach the film 3, a second thin film conductor film 8, which is formed on the film 5 and is connected to the film 3 through the above apertures 6, and a thin film resistor film 4 formed on the above substrate 1 are provided. For example, a **Ta** <SB>2</SB>N resistor film 2 and the Au conductor film 3 are continuously formed on the alumina ceramic substrate 1 to form a resistor circuit. Then, the photosensitive **polyimide** film 5 is coated and the

conductor through holes 6 for interlayer connection and a resistor trimming hole 7 are formed and cured. Then, after the second layer conductor circuit 8 is formed, the resistor pattern 4 is cut by a **laser** trimming method to adjust a resistivity.

L12 ANSWER 1 OF 23 WPIX (C) 2002 THOMSON DERWENT
AN 2002-434545 [46] WPIX
DNN N2002-342053 DNC C2002-123341
TI In-plane switching mode liquid crystal device for use in monitors for e.g., notebook computers, has two substrates, data and gate lines, data electrode(s), common electrode(s), transparent **conductive film**, and liquid crystal layer.
DC L03 P81 U14
IN LEE, J H
PA (LEEJ-I) LEE J H
CYC 1
PI US 2002044244 A1 20020418 (200246)* 10p
ADT US 2002044244 A1 US 2001-891531 20010627
PRAI KR 2000-50772 20000830
AB US2002044244 A UPAB: 20020722
NOVELTY - In-plane switching mode liquid crystal device (LCD) comprises two substrates, data and gate lines on the first substrate to define pixel regions, at least one data electrode on the first substrate, at least one common electrode on the first substrate, a transparent **conductive film** electrically connected with the common electrode, and a liquid crystal layer between the two substrates.

DETAILED DESCRIPTION - An INDEPENDENT CLAIM is included for a method for manufacturing an in-plane switching mode LCD device, which comprises providing two substrates, forming gate lines (31) and common electrodes (35) on the first substrate, forming a gate insulating film on the common electrodes, forming several data lines (33) and data electrodes (37) on the gate insulating film, forming a transparent **conductive film** (39) electrically connected with the common electrodes, and forming a liquid crystal layer between the first and second substrates.

USE - The in-plane switching mode LCD is used in monitors for notebook computers, spacecraft, and aircraft.

ADVANTAGE - The device improves response time of a liquid crystal and transmittivity by reducing the distance between the common electrode and the data electrode, and obtains a dynamic range margin of a drive **integrated circuit**. Since the transparent **conductive film** is formed between the data line and the data electrode to serve as a shielding layer, crosstalk between them can be prevented from occurring, thus improving transmittivity, luminance, and reliability.

DESCRIPTION OF DRAWING(S) - The figure is a plan view of the in-plane switching mode LCD device.
Gate line 31
Data line 33
Common electrode 35
Data electrode 37
Transparent **conductive film** 39
Contact hole 41
Dwg.3/5

L12 ANSWER 2 OF 23 WPIX (C) 2002 THOMSON DERWENT
AN 2001-209873 [21] WPIX
DNN N2001-149817
TI Semiconductor device manufacturing method for manufacture of **IC**, involves forming seed layer on adhesion/barrier layer, which includes selected alloys of copper, aluminum, gold and silver.
DC U11

IN BROWN, D; NOGAMI, T; PRAMANICK, S
PA (ADMI) ADVANCED MICRO DEVICES INC
CYC 1
PI US 6143650 A 20001107 (200121)* 6p
ADT US 6143650 A US 1999-229590 19990113
PRAI US 1999-229590 19990113
AB US 6143650 A UPAB: 20010418
NOVELTY - An adhesion/barrier layer (223) which includes selected alloys of **tantalum, titanium** and **tungsten** is formed on walls of opening formed in dielectric layer. A seed layer (224) and a **conductive layer** are formed on barrier layer which includes selected alloys of copper, aluminum, gold and silver. **Laser** annealing is done to seed layer using pulse **laser** so that seed layer and adhesion/barrier layer intermix.

DETAILED DESCRIPTION - **Laser** annealing of seed layer raises temperature of seed layer and cause intermixing of seed layer and adhesion/barrier layer. The temperature of seed layer is raised to 400 deg. C between 10-1000 nano seconds. The pulse duration of pulse **laser** used for annealing is between 1-100 nano seconds.

USE - For manufacture of **integrated circuit**.

ADVANTAGE - Enables reach of high enough temperature for optical adhesion of seed layer and barrier layer while avoiding agglomeration of copper by using **laser** pulse annealing.

DESCRIPTION OF DRAWING(S) - The figure shows the simplified cross sectional view of semiconductor after process completion.

Adhesion/barrier layer 223
Seed layer 224
Dwg.4/4

L12 ANSWER 3 OF 23 WPIX (C) 2002 THOMSON DERWENT
AN 2001-079700 [09] WPIX
DNN N2001-060658 DNC C2001-022845
TI Fabrication of a grooved fuse in **integrated circuit** applications, involves forming plug fuse in fuse via opening and simultaneously forming plugs in device area.
DC L03 U11
IN HUANG, K C; LEE, Y; LI, M; YING, T
PA (TASE-N) TAIWAN SEMICONDUCTOR MFG CO
CYC 1
PI US 6162686 A 20001219 (200109)* 12p
ADT US 6162686 A US 1998-156362 19980918
PRAI US 1998-156362 19980918
AB US 6162686 A UPAB: 20010213
NOVELTY - A grooved fuse is fabricated by forming a plug fuse in a fuse via opening and simultaneously forming plugs in a device area.

DETAILED DESCRIPTION - Fabrication of grooved fuse (58B) comprising a plug layer, involves providing a semiconductor structure having a fuse area, a guard ring area surrounding the fuse area, and a device area. A first **conductive layer** comprising first and second conductive strips is formed over the fuse area. Insulating layers having:

(i) fuse plug contacts (26) to the first (20A) and second conductive strips (20B);

(ii) device plugs in the device area; and

(iii) ring plugs in the guard ring area

are formed. The fuse plug contacts comprising non-corroding material, are electrically connected to the first and second conductive strips. A dielectric layer is formed over the insulating layers and fuse plug

contacts. A fuse via opening is etched in the dielectric layer. A plug fuse is formed in the fuse via opening, and plugs are simultaneously formed in the device area. The plug fuse is electrically connected to the fuse plug contacts. Passivation layers, metal layers and plugs are formed over the plug fuse and the dielectric layer to form device interconnects in the device area, and guard ring comprising ring plugs.

USE - For fabricating grooved fuse in **integrated circuit** applications.

ADVANTAGE - The plug fuse is formed of **tungsten** material that prevents the fuse from suffering from corrosion problem. The fuse material has a high absorbing coefficient for **laser** beam. The grooved fuse will not splash as it is burnt by a **laser**. The remaining oxide thickness on grooved fuse is controlled better during fuse window etching process. No substrate damage after **laser** repair is observed.

DESCRIPTION OF DRAWING(S) - The drawings shows cross-sectional views of the manufacture of a fuse using via plug material and surrounding guard ring.

first conductive strip 20A
second conductive strip 20B
fuse plug contacts 26
fuse 58B
Dwg.4,5/8

L12 ANSWER 4 OF 23 WPIX (C) 2002 THOMSON DERWENT
AN 2001-060271 [07] WPIX
DNN N2001-045080 DNC C2001-016642
TI Deposition of a first layer on contact hole in an insulating layer involves depositing and applying ultrasonic energy to a plate fastened with semiconductor structure.
DC L03 U11
IN LAI, H
PA (INTE-N) IND TECHNOLOGY RES INST
CYC 1
PI US 6159853 A 20001212 (200107)* 12p
ADT US 6159853 A US 1999-366738 19990804
PRAI US 1999-366738 19990804
AB US 6159853 A UPAB: 20010202

NOVELTY - A first layer is deposited by fastening a semiconductor structure with holes extending through an insulating layer to a plate in a deposition chamber; and depositing by chemical or physical vapor deposition and applying ultrasonic energy to the plate to vibrate the structure and at least partially filling the holes. The first layer is not comprised of aluminum that is sputter deposited.

DETAILED DESCRIPTION - INDEPENDENT CLAIMS are also included for (A) a method of annealing a substrate by further heating and vibrating the substrate with ultrasonic waves to flow a **conductive layer** thus filling the contact hole; and (B) a method of plating a copper layer over a substrate by further electroplating the copper layer on a barrier layer and vibrating the substrate with ultrasonic waves.

USE - For depositing a first layer on contact hole in an insulating layer using ultrasonic vibrations.

ADVANTAGE - The ultrasonic allows the layer to deposit more conformal over opening sidewalls and decreases overhangs and voids. It allows the solution to more easily diffuse in and out from the tight holes on the seed layer.

DESCRIPTION OF DRAWING(S) - The figure shows a cross sectional view

of the invention.
Insulating layer 20
Barrier layer 24
Seed layer 30
Conductive layer 34
Dwg.3/9

L12 ANSWER 5 OF 23 WPIX (C) 2002 THOMSON DERWENT
AN 2000-498607 [44] WPIX
CR 2000-463953 [38]
DNN N2000-369600 DNC C2000-149512
TI Method for customizing or repairing **integrated circuits** involves using passivated **tungsten** fuses and low-power energy beams to select which fuses are to be removed.
DC L03 U11
IN HUGGINS, A H; MACPHERSON, J
PA (CLEA-N) CLEAR LOGIC INC
CYC 1
PI US 6096566 A 20000801 (200044)* 11p
ADT US 6096566 A US 1998-64633 19980422
PRAI US 1998-64633 19980422
AB US 6096566 A UPAB: 20000913
NOVELTY - Method for customizing or repairing **integrated circuits** involves using passivated **tungsten** fuses and low-power energy beams to select which fuses are to be removed.
DETAILED DESCRIPTION - A method for customizing or repairing an **integrated circuit** comprises:
(a) forming a patterned **conductive layer** consisting of conductive lines (11) with gaps between them defining possible connection points (14) over a semiconductor substrate;
(b) depositing an insulating layer (15) on the patterned **conductive layer**;
(c) patterning and etching the insulating layer over the connection points to uncover these points;
(d) depositing a conductive metal in the connection points to form fuses (31) electrically connecting these points;
(e) forming a passivation layer (51) on top of the fuses;
(f) removing the passivation layer from at least one of the fuses; and
(g) etching the fuse(s) from which the passivation layer is removed to electrically disconnect underlying connection points.
An INDEPENDENT CLAIM is also included for a method for customizing or repairing an **integrated circuit** comprising:
(a') forming a patterned **conductive layer** consisting of conductive lines with gaps between them defining possible connection points over a semiconductor substrate;
(b') depositing an insulating layer on the patterned **conductive layer**;
(c') patterning and etching the insulating layer over the connection points to uncover these points;
(d') depositing a conductive metal in the connection points to form fuses electrically connecting these points;
(e') depositing a photoresist layer over the fuses and the insulating layer;
(f') removing the photoresist layer from at least one of the fuses; and
(g') etching the fuse(s) from which the photoresist layer is removed

to electrically disconnect underlying connection points.
USE - None given.
ADVANTAGE - Since neither precision custom masks nor high energy **laser** sources are required, the problems associated with conventional methods are reduced or eliminated. As a low energy beam is used for customizing the device, the circuit elements can be placed closer together and the device density is increased.
DESCRIPTION OF DRAWING(S) - The diagrams illustrate side views of the steps to customize an **integrated circuit** by selectively disconnecting desired connection points.
Patterned interconnect lines 10
Conductive lines 11
Vias 12
Insulating layer 13
Connection points 14
Insulating layer 15
Openings 16
Vias 17
Tungsten fuses 31
Dielectric layer 42
Openings 50
Tungsten oxide 51
Oxidized tungsten 62
2, 5, 7/9

L12 ANSWER 6 OF 23 WPIX (C) 2002 THOMSON DERWENT
AN 2000-170355 [15] WPIX
DNN N2000-126602 DNC C2000-052900
TI Reduction of **laser** mark peeling on semiconductor **wafer** edges by removing a conductive/adhesion layer which may be present over the **laser** mark but leaving a dielectric layer which may be present.
DC L03 P84 U11
IN LEE, T
PA (UNMI-N) UNITED MICROELECTRONICS CORP
CYC 1
PI US 6017662 A 20000125 (200015)* 6p
ADT US 6017662 A US 1998-181298 19981028
PRAI US 1998-181298 19981028
AB US 6017662 A UPAB: 20000323
NOVELTY - **Laser** mark peeling at the edge of a **wafer** is reduced by removing a conductive or adhesion layer which may be present over the **laser** mark but leaving a dielectric layer which may be present. Preferred **conductive layers** are polysilicon, metal silicide and metal layers; and preferred adhesion layers are **titanium nitride/titanium** layers.
USE - In providing easier reading of **laser** marks, especially alignment marks, at **wafer** edges.
DESCRIPTION OF DRAWING(S) - The drawing is a flowchart of the method for reducing **laser** mark peeling by the method of the invention.
Dwg.4/4

L12 ANSWER 7 OF 23 WPIX (C) 2002 THOMSON DERWENT
AN 2000-015477 [02] WPIX
DNN N2000-012191 DNC C2000-003393
TI Repairing opaque and clear defects of photomasks.
DC L03 P84 U11

IN GRENON, B J; HAIGHT, R A; HAYDEN, D M; HIBBS, M S; LEVIN, P J; NEARY, T E; ROCHEFORT, R A; SCHMIDT, D A; SMOLINSKI, J G; WAGNER, A; HEEPS, M S; HEIT, R A; LEVIN, J P; NIERY, T E; SCHUMIDT, D A; SMORINKSKI, J G
PA (IBMC) INT BUSINESS MACHINES CORP
CYC 26
PI EP 961168 A1 19991201 (200002)* EN 20p
R: AL AT BE CH CY DE DK ES FI FR GB GR IE IT LI LT LU LV MC MK NL PT RO SE SI
KR 99085563 A 19991206 (200056)#
KR 305488 B 20011019 (200234)#
ADT EP 961168 A1 EP 1998-303907 19980518; KR 99085563 A KR 1998-18040 19980519; KR 305488 B KR 1998-18040 19980519
FDT KR 305488 B Previous Publ. KR 99085563
PRAI EP 1998-303907 19980518; KR 1998-18040 19980519
AB EP 961168 A UPAB: 20000112
NOVELTY - A coating protects the mask during subsequent repair steps e.g., etching, **laser** ablating, focussed ion beam sputtering, **laser** beam deposition or focussed ion beam deposition. The coating may be deposited on or under chrome lines of the mask. Alternatively, a short duration **laser** pulse may be used with or without a protective coating to achieve similar results.

DETAILED DESCRIPTION - Method (A) for repairing a defect (26) on a mask (20) comprises: (a) providing a transparent substrate (24) which has a first region (22a, 22b) covered by a light absorbing first material and a second region (27) not covered by the light absorbing first material; (b) inspecting the mask and detecting an opaque defect in a defect region of the mask; (c) shining **laser** pulses on the opaque defect region to ablate the defect; using **laser** pulses of pulse duration of less than 10 picoseconds, to remove the defect without damaging the substrate underlying the defect.

An INDEPENDENT CLAIM is also included for a method (B) for repairing a defect (26) on a mask (20) comprising: (a) providing a transparent substrate (24) which has a first region (22a, 22b) covered by a light absorbing first material and a second region (27) not covered by the light absorbing first material; (b) providing a second material (40) on the second region (27) for temporarily protecting the region (27). The second material is selectively removable with respect to the first material and the substrate; (c) inspecting the mask and detecting an opaque defect in a defect region of the mask; (d) directing energy on the defect region and removing a portion of the first and second material in the defect region. An unwanted layer is deposited on the second material on the second region neighboring the defect region; and (e) selectively removing the second material and the unwanted layer.

USE - Repairing photomasks used for fabricating **integrated circuits** on semiconductor **wafers**. The process is used for repairing chromium bridge and isolated chromium defects.

ADVANTAGE - Coating comprising thin copper layer significantly improves imaging and provides more accurate control of the ion beam while protecting clear regions of the mask from FIB stain.

DESCRIPTION OF DRAWING(S) - The diagram shows top views of the steps for repairing an opaque defect.

Mask 20
First region 22a, 22b
Transparent substrate 24
Defect 26
Second region 27
Second material 40

Window 42
Clear defect 44
Dwg.2/6

L12 ANSWER 8 OF 23 WPIX (C) 2002 THOMSON DERWENT
AN 1997-261946 [24] WPIX
DNN N1997-216463 DNC C1997-084782
TI An optical semiconductor device, esp. for optical communication - has an optical waveguide and an alignment mark formed concurrently on a substrate.
DC L03 P81 U11 U12 V07
IN AOYAGI, T; MIYAZAKI, Y
PA (MITQ) MITSUBISHI DENKI KK; (MITQ) MITSUBISHI ELECTRIC CORP
CYC 4
PI GB 2307595 A 19970528 (199724)* 71p
JP 09205255 A 19970805 (199741) 18p
GB 2307595 B 19971105 (199747)
KR 97031114 A 19970626 (199828)
US 5790737 A 19980804 (199838)
US 5906753 A 19990525 (199928)
ADT GB 2307595 A GB 1996-17987 19960829; JP 09205255 A JP 1996-235472 19960905; GB 2307595 B GB 1996-17987 19960829; KR 97031114 A KR 1996-55331 19961119; US 5790737 A US 1996-695915 19960812; US 5906753 A Div ex US 1996-695915 19960812, US 1997-961145 19971030
FDT US 5906753 A Div ex US 5790737
PRAI JP 1995-303064 19951121
AB GB 2307595 A UPAB: 19971013
An optical semiconductor device consists of an optical waveguide (3) formed on a substrate (2). An alignment mark (10A) is also formed on the substrate concurrently with the waveguide.

Also claimed is a method of manufacturing an optical semiconductor device which involves first forming an optical waveguide on a substrate. An alignment mark is formed on the substrate at the same time.

Pref. a **conductive layer** is formed on the substrate with an insulating film formed on the **conductive layer**. A front surface electrode is formed on the insulating film and a back surface electrode is formed on the back surface of the substrate.

USE - For a semiconductor **laser chip**, an endface incident type photodiode or an endface incident type semiconductor amplifier which can be incorporated into an optical communication module.

ADVANTAGE - The alignment mark can be positioned precisely w.r.t. to the optical waveguide to increase the optical coupling efficiency of a communication module at a high yield.

1A,1B/27

L12 ANSWER 9 OF 23 WPIX (C) 2002 THOMSON DERWENT
AN 1997-203235 [18] WPIX
DNN N1997-167910 DNC C1997-065100
TI **Laser**-structurable doped **tin** oxide coating - for prodn. of conductor lines, esp. for sensors and circuit boards.
DC L03 P55 U14 V04 X22 X24
IN KICKELHAIN, J; VITT, B
PA (LPKF-N) LPKF CAD/CAM SYSTEME GMBH; (LPKF-N) LPKF CAD CAM SYSTEME GMBH; (LPKF-N) LPKF CAD/CAM SYSTEME GMBH FA; (LPKF-N) LPKF LASER & ELECTRONICS AG
CYC 22

PI WO 9711589 A1 19970327 (199718)* DE 15p
RW: AT BE CH DE DK ES FI FR GB GR IE IT LU MC NL PT SE
W: CN JP KR US
DE 19535068 A1 19970327 (199718) 6p
DE 19535068 C2 19970821 (199737) 6p
EP 793903 A1 19970910 (199741) DE
R: AT BE CH DE DK ES FR GB IT LI NL SE
JP 10501104 W 19980127 (199814) 16p
EP 793903 B1 19980325 (199816) DE 7p
R: AT BE CH DE DK ES FR GB IT LI NL SE
DE 59600129 G 19980430 (199823)
ES 2116817 T3 19980716 (199835)
KR 97707707 A 19971201 (199847)
JP 2931413 B2 19990809 (199937) 5p
US 5955179 A 19990921 (199945)
KR 268122 B1 20001016 (200134)
CN 1165609 A 19971119 (200148)

ADT WO 9711589 A1 WO 1996-EP4074 19960918; DE 19535068 A1 DE 1995-19535068 19950921; DE 19535068 C2 DE 1995-19535068 19950921; EP 793903 A1 EP 1996-931814 19960918, WO 1996-EP4074 19960918; JP 10501104 W WO 1996-EP4074 19960918, JP 1997-512384 19960918; EP 793903 B1 EP 1996-931814 19960918, WO 1996-EP4074 19960918; DE 59600129 G DE 1996-500129 19960918, EP 1996-931814 19960918, WO 1996-EP4074 19960918; ES 2116817 T3 EP 1996-931814 19960918; KR 97707707 A WO 1996-EP4074 19960918, KR 1997-703270 19970515; JP 2931413 B2 WO 1996-EP4074 19960918, JP 1997-512384 19960918; US 5955179 A WO 1996-EP4074 19960918, US 1997-836812 19970723; KR 268122 B1 WO 1996-EP4074 19960918, KR 1997-703270 19970515; CN 1165609 A CN 1996-191105 19960918

FDT EP 793903 A1 Based on WO 9711589; JP 10501104 W Based on WO 9711589; EP 793903 B1 Based on WO 9711589; DE 59600129 G Based on EP 793903, Based on WO 9711589; ES 2116817 T3 Based on EP 793903; KR 97707707 A Based on WO 9711589; JP 2931413 B2 Previous Publ. JP 10501104, Based on WO 9711589; US 5955179 A Based on WO 9711589

PRAI DE 1995-19535068 19950921

AB WO 9711589 A UPAB: 19970502
A coating for structured conductor line prodn. on electrically insulating substrate surfaces, esp. for prodn. of sensor elements and circuit boards, consists of a doped **tin** oxide layer of compsn. Sn1-(y+z)AyBzO2, where A is Sb or F and B is In or Al. The novelty is that the sum y + z = 0.02 to 0.11 exclusive, the ratio y/z is 1.4 to 2.2 exclusive and the coating can be structured by removal using **laser** radiation of 157-1064 nm. wavelength. Pref. the coating has the compsn. Sn0.919Sb0.052In0.029O2.

Also claimed is a method of producing the above coating by aerosol spray pyrolysis to 50-500 nm. thickness on a substrate surface at 400-600 deg. C.

USE - In the prodn. of sensors (e.g. moisture sensors for car windscreens), as well as for **microelectronic** circuits, esp. for h.f. devices on quartz glass substrates and e.g. in combination with LCD layers as displays.

ADVANTAGE - The coating can be applied as a thin, corrosion resistant, electrically **conductive coating** on glass, ceramic or semiconductor silicon substrates and can be directly **laser** beam structured in residue-free manner to form isolation channels with high resolution and extremely sharp edges.

Dwg.0/0

L12 ANSWER 10 OF 23 WPIX (C) 2002 THOMSON DERWENT
AN 1994-239522 [29] WPIX
DNN N1994-188786 DNC C1994-109792
TI Localised deposition of thin metal layers on glass or ceramic substrates - uses pref. high concentration gold resin heat treated by pref. **laser** in prescribed locations to remove or burn off resin to leave pure metal deposit.
DC L03 M13 U11 U12 U14 X15
IN PELOSCHEK, H P
PA (PELO-I) PELOSCHEK H P
CYC 1
PI NL 9202164 A 19940701 (199429)* 10p
ADT NL 9202164 A NL 1992-2164 19921214
PRAI NL 1992-2164 19921214
AB NL 9202164 A UPAB: 19940907
Method for deposition of a localised, thin metal layer of pref. gold onto a glass or ceramic material substrate in which the material deposited is a metal-organic material pref. gold resin having a high metal concentration. The deposited material is subjected in a prescribed pattern to localised heat treatment by pref. **laser** or focussed halogen lamp such that only the locations where the metal layer is required are heated. During the heat treatment of the metal-organic material, transformation occurs such that the metal is deposited and the organic remainder is burned-off or escapes in gaseous form. Following this treatment the remaining un-treated metal-organic material may be removed by e.g. rinsing or washing in a suitable solvent, together with light brushing or scrubbing, ultrasonic cleaning or similar.

USE/ADVANTAGE - For the localised deposition of metal layers, spots or small areas of e.g. gold on substrates of e.g. glass or ceramic material to form part of a circuit or for the mounting of e.g. **ICs**, or other electronic components. Can also be used for e.g. providing layers of gold on indium-**tin** oxide (ITO) conductor patterns or fluid crystal displays to enable the mounting and connection, by e.g. soldering or conducting adhesive, of the required control **ICs** using the ''**chip**-on-glass'' method. Other applications include solar cells, the deposition of metal layers for electrical connection of optically transparent, electrically **conductive layers** of automotive windscreens for e.g demisting or defrosting, and of glass or plastic windows for improved safety or security where window breakage results in electrical discontinuity. Provides a method for controlled, well defined, accurate localised metal deposition which is much simpler than comparative gas-deposition methods without the need to use gaseous, often poisonous, metal-organic materials. Heating of the deposited material is pref. by **lasers** and is therefore very localised and does not require the whole workpiece to be heated. Improves the connection of the multiple pins of **ICs** in the ''**chip**-on-glass'' method through the ability to provide localised metal deposition in the location where the **ICs** are to be mounted.
Dwg.0/0

L12 ANSWER 11 OF 23 WPIX (C) 2002 THOMSON DERWENT
AN 1992-124916 [16] WPIX
DNN N1992-093413
TI Optically measuring electrical potentials - using sensor with semiconductor exhibiting optical absorption characteristic dependent on stray electrical field.
DC S01 U11 V07

IN SOELKNER, G
PA (SIEI) SIEMENS AG
CYC 7
PI EP 480206 A 19920415 (199216)* DE 5p
R: DE FR GB IT NL
US 5164664 A 19921117 (199249) 4p
JP 04313085 A 19921105 (199251) 4p
EP 480206 A3 19930303 (199349)
ADT EP 480206 A EP 1991-115656 19910916; US 5164664 A US 1991-687180 19910418; JP 04313085 A JP 1991-287167 19911007; EP 480206 A3 EP 1991-115656 19910916
PRAI DE 1990-4032031 19901009
AB EP 480206 A UPAB: 19940126
The measuring method is based on an electro-absorption effect. It directs a **laser** probe beam (LA) onto the point (LB) at which the potential is to be measured, a measuring sensor (MS) being positioned directly over the semiconductor device (DUT).

The measuring sensor has a carrier crystal (TK) which is transparent for the **laser** beam (**TA**), carrying a transparent **conductive layer** (TL) and a mirrored dielectric semiconductor (HL), the light absorption characteristic of which is varied in dependence on the stray electrical field, resulting from the electrical potential.

USE/ADVANTAGE - High measuring accuracy for **micro-electronic** components.
1/2

L12 ANSWER 12 OF 23 WPIX (C) 2002 THOMSON DERWENT
AN 1989-000032 [01] WPIX
DNN N1989-000098
TI Thin film resistor formation on **integrated circuit wafer** - is implemented w.r.t. thicknesses and refractive indices of coatings with resistor values adjusted by **laser** trimming.
DC U11 U12
IN BAIN, A D; LANE, W A; ODWYER, T G; OLLERY, T G; RYAN, E G; COLLERY, T G
PA (ANAL-N) ANALOG RES & DEV; (ANAL-N) ANALOG RES & DEV LTD
CYC 3
PI BE 1000481 A 19881220 (198901)* 21p
LU 87352 A 19890406 (198925)
GB 2223125 A 19900328 (199013)
GB 2223125 B 19920902 (199236)
ADT BE 1000481 A BE 1988-1096 19880926; GB 2223125 A GB 1988-23626 19881007; GB 2223125 B GB 1988-23626 19881007
PRAI IE 1988-2866 19880922
AB BE 1000481 A UPAB: 19930923
Complementary MOS devices and other components are formed in an N-Si layer (4) on which a thermal oxide coating (5) is overlaid with a plasma CVD oxide layer (6). Si-Cr thin film resistors (2) are formed by sputtering or bombardment on a surface (7) of the upper oxide layer and interconnected by film conductors (11).

A plasma-enriched CVD covering of undoped SiO2 (13), derived from a gaseous mixt. of SiH4 and N2O, protects the resistors and oxide. The resistors are adjusted by pulsed **laser**-beam trimming of tabs (10), in which the creation of standing waves is avoided by suitable choice of materials.

ADVANTAGE - **Integrated circuit** devices of higher

stability can be mfd. without any need to provide doped protective layer over thin-film resistors.
1/3

L12 ANSWER 13 OF 23 WPIX (C) 2002 THOMSON DERWENT
AN 1988-331921 [47] WPIX
DNN N1988-251573 DNC C1988-146748
TI Reactive ion etching process - using gas mixt. of hydrocarbon, inert gas and hydrogen.
DC L03 U11
IN VAUDRY, C; HENRY, L
PA (ETFR) ETAT FRANCAIS; (HENR-I) HENRY L; (VAUD-I) VAUDRI C; (ETFR) FRANCE TELECOM
CYC 9
PI EP 292390 A 19881123 (198847)* FR 17p
R: CH DE GB LI NL SE
FR 2615655 A 19881125 (198903)
JP 01079389 A 19890324 (198918)
US 5074955 A 19911224 (199203)
EP 292390 B1 19940803 (199430) FR 18p
R: CH DE GB LI NL SE
DE 3850916 G 19940908 (199435)
ADT EP 292390 A EP 1988-401214 19880519; FR 2615655 A FR 1987-7135 19870521; JP 01079389 A JP 1988-122158 19880520; US 5074955 A US 1990-568871 19900817; EP 292390 B1 EP 1988-401214 19880519; DE 3850916 G DE 1988-3850916 19880519, EP 1988-401214 19880519
FDT DE 3850916 G Based on EP 292390
PRAI FR 1987-7135 19870521
AB EP 292390 A UPAB: 19930923
Reactive ion etching of III-V materials is carried out using a gas mixt. comprising (by vol.) 15-40% (exclusive) gaseous hydrocarbon(s), 20-55% (exclusive) inert gas(es) and 5-65% (exclusive) hydrogen. Pref. the gas mixt. comprises 20-30% methane, 30-50% argon and 20-50% hydrogen.

Also claimed is a process for epitaxial growth of a semiconductor layer of first III-V material on a single crystal substrate of second III-V material, in which the substrate surface is prepd., before deposition, by etching at least part of the substrate by reactive ion etching.

USE/ADVANTAGE - The process is esp. useful for etching InP, GaSb, Ga1-xInxAs, Ga1-xInxAs1-yPy, GaAs and Ga1-xAlxAs (x = 0-1; y = 0-1) in the prodn. of diodes, transistors, charge transfer devices, memories, **lasers**, photodetectors, optical guides, gratings, etc. in **microelectronics** and the telecommunications. It provides anisotropic etching and a smooth etched surface, without residues on the bottoms of the etched regions. The etched surface can be subjected directly to epitaxial semiconductor layer deposition, or insulating or **conductive layer** deposition.
11/13

L12 ANSWER 14 OF 23 WPIX (C) 2002 THOMSON DERWENT
AN 1987-022108 [03] WPIX
DNN N1987-016728 DNC C1987-009234
TI Electrically **conductive film** aggregates - comprising one or more mono molecular film layers of surface active material of liq. crystal type.
DC A85 L03 P73 U12 X12
IN VIRTANEN, J

PA (KVLI-N) K&V LICENCING OY; (KINN-I) KINNUNEN P; (KSVC-N) KSV-CHEMICALS OY
CYC 20
PI WO 8700343 A 19870115 (198703)* EN 50p
RW: AT BE CH DE FR GB IT LU NL SE
W: AU BR DK FI HU JP NO SU US
AU 8661345 A 19870130 (198716)
NO 8700836 A 19870601 (198727)
EP 228429 A 19870715 (198728) EN
R: AT BE CH DE FR GB IT LI LU NL SE
BR 8606785 A 19871013 (198746)
DK 8700958 A 19870225 (198749)
JP 62503202 W 19871217 (198805)
FI 8700676 A 19871228 (198814)
HU 46820 T 19881128 (198901)
ADT WO 8700343 A WO 1986-FI67 19860627; EP 228429 A EP 1986-904183 19860627; JP 62503202 W JP 1986-503831 19860627
PRAI FI 1985-2574 19850628; FI 1987-676 19870218
AB WO 8700343 A UPAB: 19930922
A film aggregate exhibiting electrically conducting characteristics comprises a substantially inert support surface carrying one or several monomolecular film layers, the film layer beig formed from a surface active organic material (I) having liq. crystal characteristics and having a sandwich type construction contg. (in cross section through the film) at least one following consecutive parallel zones; a spacer zone (2) which is substantially inert w.r.t. its electrical characteristics and which may contain polymerisable and/or gps. which may be bonded to the support surface; a conducting area (3-5) consisting of a charge transfer zone (3 or 5) and a polarisable zone (5 or 3) together with a spacer zone (4) between the zones (3) and (5) which is inert w.r.t. its electrical properties and which may contain polymerisable gps.; a spacer zone corresponding to zone (2) and which may also contain polymerisable gps.; and a hydrophilic zone (7) which may contain polymerisable gps.
USE/ADVANTAGE - The films can be tailor-made to give specific electrical properties, and are useful in various electronic, electric, electrochemical or photochemical applicns. such as **microcircuits**, photocells, sensors, microphones, miniature **lasers**, semiconductor **lasers**, etc., Films contg. polymerisable gps. may be used in microlithographical applicns., e.g. the film is built up on a substrate, a **micro-circuit** is drawn into the film with a **laser** or electron beam to promote polymerisation and/or bonding to the surface, and the untreated areas are removed e.g. by dissolution.
1/1

L12 ANSWER 15 OF 23 WPIX (C) 2002 THOMSON DERWENT
AN 1982-60685E [29] WPIX
TI Forming **conductive film** on diamond component - by applying metal thin layer and heat-treating using **laser** beam.
DC L02 L03 M13
PA (MATU) MATSUSHITA ELEC IND CO LTD
CYC 1
PI JP 57095895 A 19820614 (198229)* 5p
JP 61010434 B 19860329 (198617)
PRAI JP 1980-172852 19801208
AB JP 57095895 A UPAB: 19930915
Metal of **Ti**, Hf, **Ta**, Nb, Zr, Cr, Ni, Mo or **W**, an alloy thereof or a corrosion-resistant Fe alloy, e.g. stainless steel

is deposited on surface of a diamond part to form a metal thin layer. The metal thin layer is heat-treated by irradiation with a **laser** beam to form a **conductive film**. It is possible to form a **conductive film** having excellent adhesion to diamond part.

Typically a 500 micron dia cantilever comprises a **Ti** bar. A 300 micro **die** synthetic diamond particle is brazed to a tip of the **Ti** bar. The particle is mechanically ground and roughened by RF-sputter etching in 0.05 Torr O2. A 200 angstrom thick **Ti** film is formed on the rough surface of the particle by sputtering. The **Ti** film is irradiated with a **laser** beam from an Ar **laser** device to form a **conductive film**. The tip of the particle is mechanically polished to form a stylus for video disc.

L12 ANSWER 16 OF 23 WPIX (C) 2002 THOMSON DERWENT
AN 1981-32593D [18] WPIX
TI Metallised insulating substrate for communications equipment - has thin ground plane region for low power beam trimming.
DC L03 U14 W02
IN BEDARD, B E; GELLER, G R
PA (MOTI) MOTOROLA INC
CYC 11
PI WO 8101079 A 19810416 (198118)* EN
RW: AT CH DE FR GB NL SE
W: JP
US 4288530 A 19810908 (198139)
EP 37421 A 19811014 (198143) EN
R: AT CH DE FR GB LI NL SE
JP 56501149 W 19810813 (198151)
CA 1145858 A 19830503 (198323)
CA 1157958 A 19831129 (198401)
EP 37421 B 19840704 (198427) EN
R: DE FR GB NL SE
DE 3068442 G 19840809 (198433)
ADT EP 37421 A EP 1980-902196 19800915
PRAI US 1979-84941 19791015
AB WO 8101079 A UPAB: 19930915
The substrate comprises (a) a nonconductive **wafer** having conductive circuit elements on a first surface and (b) a conductive element formed on a large portion of the second surface, having a thinner portion opposite a circuit element(s) on the first surface. The appts. is tuned by trimming the thinner portion(s), as appropriate, with a low power, pref. **laser**, beam.

More specifically, the element (b) comprises (c) a (thin) **conductive layer**, (d) a second, superimposed **conductive layer**, much thicker than (c), having an aperture opposite an element(s) on the first side and (e) a third, noble metal, **conductive layer** on exposed portions of (c) and (d). The appts. is formed by photoresist masking evaporated layer (c) before plating (d), to form the aperture(s), and removing the mask before plating layer (d)..

The substrates are useful for e.g. stripline filters. The thinned, ground plane regions can be **laser** trimmed, rather than the mechanical abrasion needed for heavy plated layers, allowing automated trimming with circuitry monitored during tuning to precisely control the **laser** beam.

L12 ANSWER 17 OF 23 WPIX (C) 2002 THOMSON DERWENT
AN 1980-18381C [10] WPIX
TI Trimmable capacitor for **integrated circuit** - has high capacitance region and **laser** trimmable low capacitance region.
DC L03 U12 U13
IN REDFERN, T P
PA (NASC) NAT SEMICONDUCTOR INC
CYC 1
PI US 4190854 A 19800226 (198010)*
PRAI US 1978-877915 19780215
AB US 4190854 A UPAB: 19930902
The **integrated circuit** comprises (a) a counter electrode formed from a **conductive layer** deposited on an insulating layer on a semiconductor substrate, (b) a second insulating layer on the counter electrode, having a thin region and a thick region, (c) a first conductive electrode covering the thin region, and (d) a second conductive electrode of Si-Cr alloy, Mo-**W**, **Ta**, Ni-Cr alloy, Nb or **Ta** nitride in part of the thick insulating layer region.

The first and second electrodes are connected together and connections are made to the first and counter electrodes to form a capacitor. The capacitor value can be **laser** trimmed at the second electrode without damaging the **integrated circuit** .

Simple **laser** trimming of region having low capacitance/unit area gives precise capacitance.

L12 ANSWER 18 OF 23 JAPIO COPYRIGHT 2002 JPO
AN 1996-262475 JAPIO
TI PRODUCTION OF DISPLAY DEVICE
IN NAKAJIMA SETSUO; YAMAZAKI SHUNPEI
PA SEMICONDUCTOR ENERGY LAB CO LTD
PI JP 08262475 A 19961011 Heisei
AI JP 1995-88789 (JP07088789 Heisei) 19950321
PRAI JP 1995-88789 19950321
SO PATENT ABSTRACTS OF JAPAN (CD-ROM), Unexamined Applications, Vol. 1996
AB PURPOSE: To reduce the thickness of driver circuit parts by mechanically adhering only the semiconductor **integrated circuits** equal to stick crystals onto a substrate and electrically connecting these circuits as well.
CONSTITUTION: Metallic wirings 4 and the semiconductor **integrated circuits** 6 are mechanically fixed onto the substrate 3. Further, these circuits are electrically connected by heating the electric wirings 12 formed of materials, such as transparent **conductive films**, and metallic wirings 4 arranged on the substrate 3 to melt by irradiating the parts where both overlap on each other with a **laser**. At this time, the metallic wirings 4 are desired to melt easily. Then, low melting metals, such as aluminum, indium, **tin** and gold, are preferable. In such a case, the semiconductor **integrated circuits** 6 are formed to the structure in which N channel type TFTs 7 and P channel type TFTs 8 are held by ground surface insulating films 9, interlayer insulators 10 or passivation films 11 of silicon oxide, etc. The connection of the metallic wirings 4 and the wiring electrodes 12 may be electrically executed by fixing both with anisotropic conductive adhesives and press bonding both under heating.

L12 ANSWER 19 OF 23 JAPIO COPYRIGHT 2002 JPO
AN 1989-316968 JAPIO
TI MANUFACTURE OF **TANTALUM** THIN FILM RESISTOR
IN SUDA YASUSHI
PA NEC CORP
PI JP 01316968 A 19891221 Heisei
AI JP 1988-148763 (JP63148763 Showa) 19880615
PRAI JP 1988-148763 19880615
SO PATENT ABSTRACTS OF JAPAN (CD-ROM), Unexamined Applications, Vol. 1989
AB PURPOSE: To realize a **tantalum** thin film resistor low in resistance variation attributable to frequency changes by a method wherein on an SiO<SB>2</SB> film formed on an Si **wafer** is further covered by an insulating film wherein a β-**tantalum** thin film is converted into a **Ta**<SB>2</SB>O<SB>5</SB> film.
CONSTITUTION: An SiO<SB>2</SB> film 2 is formed on an Si **wafer** 1. Magnetron sputtering is applied for the formation of a β-**tantalum** film 3, which is next converted in a heat treatment into a **Ta**<SB>2</SB>O<SB>5</SB> film. An O<SB>2</SB>-doped **tantalum** thin film 5 is formed by magnetron sputtering, which is followed by the formation of a **conductive film** 6 consisting of an Al layer containing 1% of Si and a pure Al layer. A conductor pattern and a resistance pattern are formed, a heat treatment is accomplished for their stabilization, and then a desired resistance value is obtained by **laser** trimming. This process eliminates SiO<SB>2</SB> destruction attributable to **laser** power fluctuation. In this way, a **tantalum** thin film resistor, low in resistance variation attributable to changes in frequency, may be obtained.
COPYRIGHT: (C)1989,JPO&Japio

L12 ANSWER 20 OF 23 JAPIO COPYRIGHT 2002 JPO
AN 1985-041252 JAPIO
TI MANUFACTURE OF HYBRID **INTEGRATED CIRCUIT**
IN HARADA KEIJI
PA NEC CORP
PI JP 60041252 A 19850304 Showa
AI JP 1983-149894 (JP58149894 Showa) 19830817
PRAI JP 1983-149894 19830817
SO PATENT ABSTRACTS OF JAPAN (CD-ROM), Unexamined Applications, Vol. 1985
AB PURPOSE: To improve the absolute accuracy of a resistor and temperature characteristic and to reduce the size by printing a thin **film conductive** paste on a substrate, baking it and then forming a film to be partly superposed with a thick film conductor pattern on the thin film for a resistor.
CONSTITUTION: A silver-palladium paste is printed on an aluminum substrate 1, and baked to form a thick film conductor pattern 2. An oxygen-doped nitrided **tantalum** film 3 is formed on the entire surface of a structure. The film 3 is etched with a mixture solution of hydrofluoric acid, nitric acid and acetic acid so as to become part of a thick film conductor by photolithographic technique, the resistor is stabilized and heat treated, and cut at the part 4 by a **laser** trimming method, thereby obtaining a desired resistance value.
COPYRIGHT: (C)1985,JPO&Japio

L12 ANSWER 21 OF 23 JAPIO COPYRIGHT 2002 JPO
AN 1985-041251 JAPIO

TI MANUFACTURE OF HYBRID **INTEGRATED CIRCUIT**
IN HARADA KEIJI
PA NEC CORP
PI JP 60041251 A 19850304 Showa
AI JP 1983-149893 (JP58149893 Showa) 19830817
PRAI JP 1983-149893 19830817
SO PATENT ABSTRACTS OF JAPAN (CD-ROM), Unexamined Applications, Vol. 1985
AB PURPOSE: To improve the absolute accuracy of a resistor and the temperature characteristic and to reduce the size by forming a pattern of a thin film for a resistor and printing a thick **film conductive** paste to be partly superposed on the thin film for the resistor.
CONSTITUTION: An oxygen-doped nitrided **tantalum** film 2 is formed on an aluminum substrate 1 in a magnetron sputtering device. The film 2 is etched, a copper paste 3 is then printed by a screen printing method so as to be partly superposed with part of the film 2, and baked in a nitrogen atmosphere. After baking, part 4 of the resistor is cut by a **laser** trimming method, thereby obtaining a desired resistance value.

L12 ANSWER 22 OF 23 JAPIO COPYRIGHT 2002 JPO
AN 1984-019259 JAPIO
TI COATED TYPE INFORMATION RECORDING DISC
IN HIRANO SHOJI; MATSUNO KUNIO; SANBE HIDEO; KISHIMOTO TAIICHI
PA TOSHIBA CORP
PI JP 59019259 A 19840131 Showa
AI JP 1982-126692 (JP57126692 Showa) 19820722
PRAI JP 1982-126692 19820722
SO PATENT ABSTRACTS OF JAPAN (CD-ROM), Unexamined Applications, Vol. 1984
AB PURPOSE: To increase the signal output and CNR in the stage of reproduction and to enable the stable and easy production of a titled disc by forming a dielectric layer only on the surface of a **conductive layer** by chemical reaction.
CONSTITUTION: 3pt.wt. a **tin** stabilizer, and butyl stearate are mixed and kneaded with 100pts.wt. PVC, and the mixture is cut to obtain pellets. The pellets are molded under pressure at 185∼190°C molding temp. by using **dies** consisting of a master produced by recording video signals by a **laser** beam on photoresist, whereby a substrate 12 of a disc shape (26cm diameter, 1.2mm thickness) is obtd. An Ni layer 13 of 500Å thickness is formed by sputtering on the surface thereof. The part of the Ni layer 13 made in such a way is dipped for five minutes in potassium dichromate (5wt%) to oxidize the surface, whereby a dielectric layer 14 is formed and a coated type information recording disc 11 is prepd.

L12 ANSWER 23 OF 23 JAPIO COPYRIGHT 2002 JPO
AN 1984-006587 JAPIO
TI SEMICONDUCTOR **LASER** DEVICE
IN MATSUEDA HIDEAKI; NAKAMURA MICHIHARU
PA AGENCY OF IND SCIENCE & TECHNOL
PI JP 59006587 A 19840113 Showa
AI JP 1982-115341 (JP57115341 Showa) 19820705
PRAI JP 1982-115341 19820705
SO PATENT ABSTRACTS OF JAPAN (CD-ROM), Unexamined Applications, Vol. 1984
AB PURPOSE: To make electrical connection between both sufficient in case of integration of a **laser** diode with an electrical circuit in a

lateral direction, and reduce the floating capacity, further offer an integration structure whereby the pattern formation of a complicated and precise electrical circuit can be attained.
CONSTITUTION: The titled device is an example applied for an **integrated circuit** wherein GaAs/GaAlAs is used, and composed of a semi-insulating GaAs substrate 1, an N-GaAs **conductive layer** 2, an N-GaAlAs clad layer 3, a P-GaAs cap layer 6, bonding pads (Cr/Au) 8, 13, 14, a **laser** stripe electrode (Cr/Au)G, ohmic electrodes (AuGe/Ni/Au) 10, 12, a Schottky electrode (**Ti**/Tt/Au) 11 and an SiO<SB>2</SB> film 15. A thickened active layer oscillates **laser** at the active region of a TS **laser**.

FILE 'REGISTRY' ENTERED AT 11:39:42 ON 13 SEP 2002

L1 74887 S PA/PCT
L2 46850 S PI/PCT
L3 733753 S AYS/CI
E POLYCYCLIC AROMATIC HYDROCARBON/CN
L4 1 S "POLYCYCLIC AROM. HYDROCARBONS"/CN
L5 1 S POLYANILINE/CN

FILE 'HCAPLUS, INSPEC' ENTERED AT 11:42:06 ON 13 SEP 2002

L6 72163 S (B220 OR B2570)/CC
L7 758046 S LASER OR IRASER OR QUANTUM(W) GENERATOR
L8 2841 S B4320/CC
L9 1068220 S TAN OR TA OR TIN OR TI OR W OR WN OR TASIN
L10 109211 S ((TANTALUM OR TITANIUM OR TUNGSTEN)(N)(NITR
L11 215931 S POLYIMIDE OR POLYAMIDE OR POLYARLYENE OR
L12 537405 S IC OR ICS OR ((INTEGRATED OR LOGIC)(W)(CIRC
L13 546601 S L6 OR L12
L14 23406 S L13 AND L7
L15 0 S L5(L) CONDUCITIV?
L16 449 S L14 AND (L1 OR L2 OR L4 OR L5 OR L11)
L17 48 S L16 AND (L9 OR L10)
L18 7 S L16 AND (CONDUCTIV?)(N)(FILM OR LAYER? OR
L19 89 S L16 AND (WIRE OR LINE)
L20 81 S (L18 OR L19) NOT L17
L21 70 DUP REMOVE L20 (11 DUPLICATES REMOVED)
L22 121 S L16 AND (WIR### OR LIN###)
L23 28 S L22 AND (OXIDE OR DIELECTRIC OR INSULAT?)(2
N)(LAYER? OR FILM OR COAT####)
L24 29 S (L23 OR L18) NOT L17

```
     FILE 'REGISTRY' ENTERED AT 10:23:10 ON 13 SEP 2002
L1        74878 S PA/PCT
L2        46845 S PI/PCT
L3       733618 S AYS/CI
                E POLYCYCLIC AROMATIC HYDROCARBON/CN
L4            1 S E2
L5            1 S POLYANILINE/CN

     FILE 'HCAPLUS' ENTERED AT 10:26:07 ON 13 SEP 2002

     FILE 'HCAPLUS, INSPEC' ENTERED AT 10:26:36 ON 13 SEP 2002
L6        72163 S (B220 OR B2570)/CC
L7       758046 S LASER OR IRASER OR QUANTUM(W)GENERATOR
L8         2841 S B4320/CC
L9      1068220 S TAN OR TA OR TIN OR TI OR W OR WN OR TASIN OR TISIN OR TA()N
L10      619406 S ((TANTALUM OR TITANIUM OR TUNGSTEN)(N)(NITRIDE)) OR TANTALUM
L11      215931 S POLYIMIDE OR POLYAMIDE OR POLYARLYENE OR POLYARYLENE OR (POLY
L12      537405 S IC OR ICS OR ((INTEGRATED OR LOGIC)(W)(CIRCUIT)) OR (MICRO)(W
L13      546601 S L6 OR L12
L14       23406 S L13 AND L7
L15           0 S L5(L)CONDUCITIV?
L16         449 S L14 AND (L1 OR L2 OR L4 OR L5 OR L11)
L17          58 S L16 AND (L9 OR L10)
L18          48 DUP REMOVE L17 (10 DUPLICATES REMOVED)
```

L18 ANSWER 1 OF 48 HCAPLUS COPYRIGHT 2002 ACS
AN 2002:502791 HCAPLUS
DN 137:55987
TI Self-aligned fuse structure and method with dual-thickness dielectric
IN Giust, Gary K.; Castagnetti, Ruggero; Liu, Yauh-ching; Ramesh, Subramanian
PA Lsi Logic Corporation, USA
SO U.S., 11 pp., Division of U.S. Ser. No. 118,231.
CODEN: USXXAM
DT Patent
LA English
FAN.CNT 1

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	US 6413848	B1	20020702	US 2000-534907	20000323
PRAI	US 1998-118231	A3	19980717		

AB The invention relates to a self-aligned semiconductor fuse structure in a semiconductor memory device. The fuse break point, that point at which the elec. link of which the fuse is part is severed by a **laser** beam, is self-aligned by the use of photolithog. patterned anti-reflective dielec. coatings. The self-alignment allows the size location of the break point to be less sensitive to the **laser** beam size and alignment. This has several advantages including allowing photolithog. control and effective size redn. of the **laser** spot irradiating the fuse material and surrounding structure. This permits reduced fuse pitch, increasing d. and the efficiency of use of **chip** area, and results in reduced thermal exposure, which causes less damage to **chip**. In addn., **laser** alignment is less crit. and therefore less timely, which increases throughput in fabrication.
RE.CNT 22 THERE ARE 22 CITED REFERENCES AVAILABLE FOR THIS RECORD
ALL CITATIONS AVAILABLE IN THE RE FORMAT

L18 ANSWER 2 OF 48 HCAPLUS COPYRIGHT 2002 ACS
AN 2002:6715 HCAPLUS
DN 136:78260
TI Semiconductor flip-**chip** package
IN Capote, Miguel Albert; Zhu, Xiaoqi; Burress, Robert Vinson; Lee, Yong-joon
PA USA
SO U.S., 21 pp., Cont.-in-part of U.S. 6,297,560.
CODEN: USXXAM
DT Patent
LA English
FAN.CNT 4

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	US 6335571	B1	20020101	US 2000-517839	20000302
	US 5985043	A	19991116	US 1997-897968	19970721
	US 5985456	A	19991116	US 1997-926159	19970909
	US 6017634	A	20000125	US 1998-12382	19980123
	US 6121689	A	20000919	US 1998-120172	19980721
	US 6297560	B1	20011002	US 1998-137971	19980821
	US 2002014703	A1	20020207	US 2001-935432	20010820
	US 2002031868	A1	20020314	US 2001-948921	20010907
	US 6399426	B1	20020604		
PRAI	US 1997-53407P	P	19970721		
	US 1997-897968	A1	19970721		

US 1997-56043P P 19970902
US 1997-926159 A1 19970909
US 1998-12382 A1 19980123
US 1998-120172 A2 19980721
US 1998-137971 A2 19980821
US 1996-28796P P 19961031
US 2000-517839 A3 20000302

AB A flip-**chip** device and process for fabricating the device employs a multilayer encapsulant that includes a 1st portion encapsulant having a coeff. of thermal expansion of .ltoreq.30 ppm/.degree. and an elastic modulus of 2-20 GPa and a 2nd portion comprising a polymer flux having a coeff. of thermal expansion that may exceed 30 ppm/.degree..

RE.CNT 20 THERE ARE 20 CITED REFERENCES AVAILABLE FOR THIS RECORD
ALL CITATIONS AVAILABLE IN THE RE FORMAT

L18 ANSWER 3 OF 48 HCAPLUS COPYRIGHT 2002 ACS
AN 2001:904597 HCAPLUS
DN 136:17684
TI Integrated active flux microfluidic devices and methods
IN Quake, Stephen R.; Chou, Hou-pu
PA California Institute of Technology, USA
SO PCT Int. Appl., 177 pp.
CODEN: PIXXD2
DT Patent
LA English
FAN.CNT 2

PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
WO 2001094635	A2	20011213	WO 2001-US18400	20010605

W: AE, AG, AL, AM, AT, AU, AZ, BA, BB, BG, BR, BY, BZ, CA, CH, CN, CO, CR, CU, CZ, DE, DK, DM, EC, EE, ES, FI, GB, GD, GE, HR, HU, ID, IL, IN, IS, JP, KE, KG, KP, KR, KZ, LC, LK, LR, LS, LT, LU, LV, MA, MD, MG, MK, MN, MW, MX, MZ, NO, NZ, PL, PT, RO, RU, SD, SE, SG, SI, SK, SL, TJ, TM, TR, TT, TZ, UA, UG, US, UZ, VN, YU, ZA, ZW, AM, AZ, BY, KG, KZ, MD, RU, TJ, TM
RW: GH, GM, KE, LS, MW, MZ, SD, SL, SZ, TZ, UG, ZW, AT, BE, CH, CY, DE, DK, ES, FI, FR, GB, GR, IE, IT, LU, MC, NL, PT, SE, TR, BF, BJ, CF, CG, CI, CM, GA, GN, GW, ML, MR, NE, SN, TD, TG

PRAI US 2000-209243P P 20000605
US 2000-211309P P 20000613
US 2000-249360P P 20001116
US 2000-724548 A2 20001128

AB The invention relates to a microfabricated device for the rapid detection of DNA, proteins or other mols. assocd. with a particular disease. The devices and methods of the invention can be used for the simultaneous diagnosis of multiple diseases by detecting mols. (e.g. amts. of mols.), such as polynucleotides (e.g., DNA) or proteins (e.g., antibodies), by measuring the signal of a detectable reporter assocd. with hybridized polynucleotides or antigen/antibody complex. In the microfabricated device according to the invention, detection of the presence of mols. (i.e., polynucleotides, proteins, or antigen/antibody complexes) are correlated to a hybridization signal from an optically-detectable (e.g. fluorescent) reporter assocd. with the bound mols. These hybridization signals can be detected by any suitable means, for example optical, and can be stored for example in a computer as a representation of the presence of a particular gene. Hybridization probes can be immobilized on a substrate that forms part of or is exposed to a channel or channels of

the device that form a closed loop, for circulation of sample to actively contact complementary probes. Universal **chips** according to the invention can be fabricated not only with DNA but also with other mols. such as RNA, proteins, peptide nucleic acid (PNA) and **polyamide** mols.

L18 ANSWER 4 OF 48 HCAPLUS COPYRIGHT 2002 ACS
AN 2001:851773 HCAPLUS
DN 135:379722
TI **Wafer**-scale assembly of **chip**-size packages
IN Heinen, Katherine G.; Edwards, Darvin R.; Jacobs, Elizabeth G.
PA USA
SO U.S. Pat. Appl. Publ., 17 pp.
CODEN: USXXCO
DT Patent
LA English
FAN.CNT 1

PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
US 2001044197	A1	20011122	US 1998-186973	19981105

AB A **wafer**-scale assembly app. for **integrated circuits** and a method for forming the **wafer**-scale assembly are disclosed. A semiconductor **wafer** including a plurality of circuits is provided with a plurality of metal contact pads as elec. entry and exit ports. A 1st **wafer**-scale patterned polymer film carrying solder balls for each of the contact pads on the **wafer** is positioned opposite the **wafer** and the film are aligned. The film is brought into contact with the **wafer**. Radiant energy in the near IR spectrum is applied to the backside of the **wafer**, heating the **wafer** uniformly and rapidly without moving the semiconductor **wafer**. Thermal energy is transferred through the **wafer** to the surface of the **wafer** and into the solder balls, which reflow onto the contact pads, while the thermal stretching of the polymer film is mech. compensated. The uniformity of the height of the liq. solder balls is controlled either by mech. stoppers or by the precision linear motion of motors. After cooling, the solder balls solidify and the 1st polymer film is removed. The process is repeated for assembling sequentially a **wafer**-scale patterned interposer overlying all of the solder balls and the **wafer** and contacting each solder ball with a soldered joint, and a 2nd **wafer** -scale patterned film carrying solder balls contacting the interposer. In each process, the **wafer** is heated uniformly and rapidly and without moving it, the alignment is maintained during heating by mech. compensating for the thermal stretching of the polymer film, and the uniformity of the height of the liq. solder balls is controlled by mech. stoppers or position closed-loop linear actuators. The 2nd film is removed after cooling. Other embodiments are also disclosed.

L18 ANSWER 5 OF 48 HCAPLUS COPYRIGHT 2002 ACS
AN 2001:703763 HCAPLUS
DN 135:235008
TI Process for controlling oxide thickness over a fusible link using transient etch stops
IN Tzeng, Wen-Tsing; Chen, Yue-Feng; Wang, Kau-Jan
PA Vanguard International Semiconductor Corporation, Taiwan
SO U.S., 11 pp.
CODEN: USXXAM

DT Patent
LA English
FAN.CNT 1

PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
US 6294474	B1	20010925	US 1999-425906	19991025

AB A method is described for progressively forming a fuse access opening for **laser** trimming in an **integrated circuit** with improved control of dielec. thickness over the fuse. A dielec. layer is formed over the fuse and a polysilicon layer is then patterned over the fuse to form a 1st etch stop. An inter-level dielec. (ILD) layer is added and a 2nd etch stop is formed in a 1st metal layer on the ILD layer over the 1st etch stop. The 2nd etch stop serves to protect the ILD layer over the fuse from being etched by an ARC over etch during the via etching in a 1st inter-metal dielec. (IMD) layer. A 1st portion of the **laser** access window is formed during the via etching of the 1st IMD layer. The 2nd etch stop is then removed by the 2nd metal patterning etch, exposing the ILD layer over the 1st etch stop at it's original thickness. A passivation layer is deposited and patterned to form access openings to bonding pads as well as to further open the **laser** access window to the 1st etch stop. The 1st etch stop prevents penetration of the subjacent insulative layer over the fuse, thereby maintaining a controlled uniform thickness of that layer. When the bonding pads are opened, including the removal of an ARC on their surface, the etchant conditions are changed to remove the etch stop and subsequently a portion of the subjacent insulative layer over the fuse leaving a precise and uniform thickness of dielec. material over the fuse. The process fits conveniently within the framework of an existing process and does not introduce any addnl. steps.

RE.CNT 8 THERE ARE 8 CITED REFERENCES AVAILABLE FOR THIS RECORD
ALL CITATIONS AVAILABLE IN THE RE FORMAT

L18 ANSWER 6 OF 48 HCAPLUS COPYRIGHT 2002 ACS
AN 2001:502474 HCAPLUS
DN 135:85596
TI Self-aligned fuse structure with increased density and reduced thermal exposure and method of fabrication with heat sink
IN Giust, Gary K.; Castagnetti, Ruggero; Liu, Yauh-ching; Ramesh, Subramanian
PA Lsi Logic Corporation, USA
SO U.S., 14 pp.
CODEN: USXXAM
DT Patent
LA English
FAN.CNT 1

PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
US 6259146	B1	20010710	US 1998-118232	19980717

AB Provided are a self-aligned semiconductor fuse structure, a method of making such a fuse structure, and apparatuses incorporating such a fuse structure. The fuse break point, that point at which the elec. link of which the fuse is part is severed by a **laser** beam, is self-aligned using photolithog. patterned dielec. and a heat sink material. The self-alignment allows the size and location of the break point to be more forgiving of the **laser** beam size and alignment. This has several advantages, including allowing photolithog. control and effective size redn. of the **laser** spot irradiating the fuse material and surrounding structure. This permits reduced fuse pitch,

increasing d. and the efficiency of use of **chip** area, and results in reduced thermal exposure, which causes less damage to **chip**. In addn., **laser** alignment is less crit. and therefore less time-consuming, which increases throughput in fabrication. The present invention exploits the characteristic of most dielec. materials that they are poor conductors of thermal energy. Thermal resistance increases with the thickness of the dielec. Thus that heat is conducted more easily and thus quickly through a relatively thin portion of dielec. than it is through a relatively thick portion of dielec. In alternative embodiments, the present invention also exploits the characteristic of a dielec. material that its reflectance changes with its thickness due to optical interference effects. In such embodiments, the self-alignment of the fuse break point is further facilitated using photolithog. and anti-reflective coatings.

RE.CNT 20 THERE ARE 20 CITED REFERENCES AVAILABLE FOR THIS RECORD
ALL CITATIONS AVAILABLE IN THE RE FORMAT

L18 ANSWER 7 OF 48 HCAPLUS COPYRIGHT 2002 ACS
AN 2001:366761 HCAPLUS
DN 134:360263
TI Integrated high-performance decoupling capacitor and heat sink
IN Bernstein, Kerry; Geffken, Robert M.; Pricer, Wilbur D.; Stamper, Anthony K.; Voldman, Steven H.
PA International Business Machines Corp., USA
SO U.S., 10 pp.
CODEN: USXXAM
DT Patent
LA English
FAN.CNT 1

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	US 6236103	B1	20010522	US 1999-283828	19990331
	US 2001050408	A1	20011213	US 2001-764504	20010117
PRAI	US 1999-283828	A3	19990331		

AB A significant and very effective decoupling capacitor and heat sink combination that, in a single structure provides both a heat sink and a decoupling capacitor in close proximity to the active circuit on the **chip** requiring either heat sinking or decoupling capacitance or both. This is achieved by forming on a semiconductor **chip**, having a buried oxide layer therein, an integrated high-performance decoupling capacitor that uses a metallic deposit >30 .mu. thick formed on the back surface of the **chip** and elec. connected to the active **chip** circuit to result in a significant and very effective decoupling capacitor and heat sink in close proximity to the active circuit on the **chip** requiring such decoupling capacitance and heat sinking capabilities. The decoupling capacitance can use the substrate of the **chip** itself as 1 of the capacitive plates and a formed metallic deposit as the second capacitive plate which also serves as a heat sink for the active circuit formed in the **chip**. The structure thus provides both a significant and effective decoupling capacitance in close proximity to the active circuit on the **chip** requiring such decoupling capacitance as well as providing improved heat sinking for the decoupled active circuit.

RE.CNT 3 THERE ARE 3 CITED REFERENCES AVAILABLE FOR THIS RECORD
ALL CITATIONS AVAILABLE IN THE RE FORMAT

L18 ANSWER 8 OF 48 HCAPLUS COPYRIGHT 2002 ACS

AN 2001:331257 HCAPLUS
DN 134:319848
TI Flip **chip** having integral mask and underfill providing two-stage bump formation
IN Gilleo, Kenneth Burton; Blumel, David
PA Fry's Metals, Inc., USA
SO U.S., 8 pp., Cont.-in-part of U.S. Ser. No. 266,166.
CODEN: USXXAM
DT Patent
LA English
FAN.CNT 4

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	US 6228681	B1	20010508	US 1999-395558	19990914
	US 6228678	B1	20010508	US 1999-266166	19990310
PRAI	US 1999-266166	A2	19990310		
	US 1998-67381	A2	19980427		

AB The present invention relates to a process for forming a two-stage bump on a flip **chip**. The process employs an underfill material which can be formed to act as a mask for application of bumps formed from a 1st compn. to the flip **chip**. A material having a different compn. can then be applied to the bumps.
RE.CNT 4 THERE ARE 4 CITED REFERENCES AVAILABLE FOR THIS RECORD
ALL CITATIONS AVAILABLE IN THE RE FORMAT

L18 ANSWER 9 OF 48 HCAPLUS COPYRIGHT 2002 ACS
AN 2001:73502 HCAPLUS
DN 134:124771
TI Passivation layer etching process for memory arrays with fusible links
IN Tzeng, Wen-Tsing; Yang, Chun-Pin; Lin, Hsing-Lien
PA Vanguard International Semiconductor Corporation, Taiwan
SO U.S., 17 pp.
CODEN: USXXAM
DT Patent
LA English
FAN.CNT 1

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	US 6180503	B1	20010130	US 1999-354852	19990729

AB A method is described for progressively forming a fuse access openings in **integrated circuits** which are built with redundancy and use **laser** trimming to remove and insert circuit sections. The fuses are formed in a polysilicon layer and covered by .gtoreq.1 relatively thin insulative layers. An etch stop is patterned over the fuse in a higher level polysilicon layer or a 1st metalization layer. Addnl. insulative layers such as inter-metal dielec. layers are then formed over the etch stop. A 1st portion of the **laser** access window is then etched during the via etch for the top metalization level. The etch stop prevents removal of the insulation subjacent to it. Cumulative thickness non-uniformities in the relatively thick upper insulative layers are thus removed from the fuse window. The etch stop is removed during patterning of the top level metalization. A passivation layer is applied and patterned to exposed bonding pads and, at the same time complete the etching of the **laser** access window to a desired thickness over the fuses. The passivation layer over etch required to penetrate the insulation layer over the fuses also removes an antireflective coating over the bonding pads. The process fit

conveniently within the framework of an existing process and does not introduce any addnl. steps. In addn., the passivation layer can be patterned to form final access to both bonding pads and **laser** access openings with a single photolithog. mask.

RE.CNT 15 THERE ARE 15 CITED REFERENCES AVAILABLE FOR THIS RECORD
ALL CITATIONS AVAILABLE IN THE RE FORMAT

L18 ANSWER 10 OF 48 HCAPLUS COPYRIGHT 2002 ACS
AN 2002:350373 HCAPLUS
DN 137:162929
TI A **laser**-polymerized thin film silica surface modification for suppression of cell adhesion and electroosmotic flow in microchannels
AU Kirby, Brian J.; Wheeler, Aaron R.; Shepodd, Timothy J.; Fruetel, Julia A.; Hasselbrink, Ernest F.; Zare, Richard N.
CS Sandia National Laboratories, Livermore, CA, 94551-0969, USA
SO Micro Total Analysis Systems 2001, Proceedings .mu.TAS 2001 Symposium, 5th, Monterey, CA, United States, Oct. 21-25, 2001 (2001), 605-606. Editor(s): Ramsey, J. Michael; Berg, Albert van den. Publisher: Kluwer Academic Publishers, Dordrecht, Neth.
CODEN: 69COT6; ISBN: 1-4020-0148-7
DT Conference
LA English
AB A **laser**-polymd. thin film for silica surface modification is presented. This technique enables photopatterned surface charge modification consistent with optical tweezer techniques. This charge modification may be applied for **chip**-based cell techniques and multi-dimensional sepn. techniques that require nonuniform zeta potential on a microfluidic **chip**.

RE.CNT 1 THERE ARE 1 CITED REFERENCES AVAILABLE FOR THIS RECORD
ALL CITATIONS AVAILABLE IN THE RE FORMAT

L18 ANSWER 11 OF 48 INSPEC COPYRIGHT 2002 IEE
AN 2002:7274113 INSPEC DN B2002-06-2250-007
TI Process for fabricating dense, **chips**-first MCMs with thinned **die**.
AU LeBlanc, J.J.; Tumminelli, R.P.; Singleton, M.C.; Ayers, E.P.; Haley, J.F.; Ives, G.V.; Dineen, A.D. (Electron. Packaging & Prototyping Div., Draper (C.S.) Lab., Cambridge, MA, USA)
SO Proceedings 2001 HD International Conference on High-Density Interconnect and Systems Packaging (SPIE Vol.4428)
Washington, DC, USA: IMAPS - Int. Microelectron. & Packaging Soc, 2001. p.364-8 of x+380 pp. 5 refs.
Conference: Santa Clara, CA, USA, 17-20 April 2001
Sponsor(s): IMAPS - Int. Microelectron. & Packaging Soc.; CMP Media; SPIE
ISBN: 0-930815-63-7
DT Conference Article
TC Practical; Experimental
CY United States
LA English
AB There is a continual push in the **microelectronic** industry for denser packaging both in terms of footprint area and total volume. We present a robust process for fabricating **chips** first multi-**chip** modules (MCMs). The process incorporates the use of **die** that are thinned to six mils and subsequently placed to within 130 mu m (0.005") of each other. The placement accuracy is +or-13 mu m (0.0005") and can be maintained through curing. This allows us to use fixed drill files and masks with 75 mu m (0.003") capture pads. The six

mil **die** are surrounded with a **polyimide** windowpane to create a planar surface on which to construct the interconnect. A **polyimide** dielectric layer is then laminated on top of the **die**, blind vias are **laser** drilled to the **die**, and a **Ti**/Cu/**Ti** interconnect structure is then built over the **die**. Subsequent layers are then built up, with the interconnect residing above the **die**. When modules are diced out, the overall area is only slightly larger than the combined area of the **die**. Total module thickness for a four level module is typically 560 mu m (0.022"). We also present thermal shock data for our interconnect structure.

L18 ANSWER 12 OF 48 HCAPLUS COPYRIGHT 2002 ACS
AN 2001:294562 HCAPLUS
DN 135:84014
TI Patterning, electroplating and removal of SU 8 molds by excimer **laser** micromachining
AU Ghantasala, Muralidhar K.; Hayes, Jason P.; Harvey, Erol C.; Sood, Dinesh K.
CS Industrial Research Institute Swinburne, Swinburne University of Technology, Victoria, 3122, Australia
SO Journal of Micromechanics and Microengineering (2001), 11(2), 133-139
CODEN: JMMIEZ; ISSN: 0960-1317
PB Institute of Physics Publishing
DT Journal
LA English
AB The ablation characteristics of the SU 8 photoresist (spun on Si **wafers**) under 248 KrF excimer pulsed **laser** radiation were studied. The variation of etch rate with fluence was studied in the range 0.05-3.01 J cm-2. The threshold fluence for ablation of SU 8 is .apprx.0.05 J cm-2. The etch rate of SU 8 is higher than that of **polyimide** (previously reported) under similar conditions. The authors have studied the effects of different prebake temps. (90, 110, 120 and 200.degree.) on ablation characteristics, which are similar for all temps. The effect of increasing the no. of **laser** shots (from 10 to 10000) was examd. at different fluences to understand the etch-rate variation near the 'end of film' stage of ablation. The results of the authors' anal. using SEM, profilometry and optical microscopy reveal the very smooth morphol. of the etched surfaces with no significant debris, no noticeable damage to underlying Si and the gradual build-up of a carbonaceous film outside and around the etch pits. The authors find SU 8 very suitable for excimer ablation lithog. and demonstrated this by patterning a gear structure in an SU 8 resist layer with an aspect ratio of 4.5. For the 1st time, the **laser** micromachining technique has the potential to cleanly remove SU 8 after electroplating a microstructure with Cu.
RE.CNT 22 THERE ARE 22 CITED REFERENCES AVAILABLE FOR THIS RECORD
ALL CITATIONS AVAILABLE IN THE RE FORMAT

L18 ANSWER 13 OF 48 HCAPLUS COPYRIGHT 2002 ACS
AN 2002:138479 HCAPLUS
DN 136:301467
TI Integration of CMOS process-compatible optoelectronic interconnects for high-speed communications
AU Chen, Ray T.; Zhang, Xuping; Liu, Yujie; Lin, Lei; Choi, G.
CS Microelectronics Research Center, Department of Electrical and Computer Engineering, University of Texas at Austin, Austin, TX, 78758, USA

SO Proceedings of SPIE-The International Society for Optical Engineering (2001), 4602(Semiconductor Optoelectronic Device Manufacturing and Applications), 23-27
CODEN: PSISDG; ISSN: 0277-786X
PB SPIE-The International Society for Optical Engineering
DT Journal
LA English
AB The design and integration of a fully embedded Si-CMOS process-compatible optical interconnects are presented. The transmitting and receiving functions will be incorporated within the embedded optoelectronic interconnection layers of 3-dimensional integrated multilayer boards and ASICs. All elements including waveguide, coupler, detector and **laser** for the fully embedded board-level optical interconnection system are developed. The propagation loss of waveguide is 0.58 dB/cm at 632.8 nm and 0.21 dB/cm at 850 nm. The 45-degree TIR (total internal reflection) micro-mirror couplers with high coupling efficiencies are formed by reactive ion etching. The MSM (metal-semiconductor-metal) photo-detector array is fabricated on a GaAs **wafer** by a CMOS compatible technique. The external quantum efficiency of 0.4 A/**W** and 3 dB bandwidth of the integrated MSM photo-detector of 2.648 GHz are exptl. confirmed. The VCSEL array with a sacrificial layer for the epitaxial liftoff of VCSEL from the GaAs substrate is designed and manufd. A 1 X 12 array of VCSELs, MSM photodetectors and **polyimide** channel waveguides via 45-degree TIR micro-couplers are integrated on Si **wafer**. The exptl. performances of the highly integrated system are given.

L18 ANSWER 14 OF 48 HCAPLUS COPYRIGHT 2002 ACS
AN 2000:314966 HCAPLUS
DN 132:316633
TI Adhesion-promoting layer for generating conductor structures with good adhesive properties on insulating material used in electronics
IN Kickelhain, Jorg; Vitt, Bruno
PA LPKF Laser & Electronics A.-G., Germany
SO PCT Int. Appl., 17 pp.
CODEN: PIXXD2
DT Patent
LA German
FAN.CNT 1

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	WO 2000027175	A1	20000511	WO 1999-DE3465	19991029
	W: JP, US				
	RW: AT, BE, CH, CY, DE, DK, ES, FI, FR, GB, GR, IE, IT, LU, MC, NL, PT, SE				
	DE 19850592	C1	20001012	DE 1998-19850592	19981103
PRAI	DE 1998-19850592	A	19981103		

AB The invention relates to a thin, chem. metalizable metal oxide-based adhesion-promoting layer for insulating material for producing conductor structures with good adhesive properties by **laser** radiation. The adhesion-promoting layer has a thickness of 20-200 nm and has an O concn. in a layer area adjacent to the insulating material that continuously decreases from a max. value at the insulating material to the value zero as the distance from the insulating material increases. In the layer area with decreasing O concn., the adhesion-promoting layer comprises as metals Cu, Cr, Ni, **Ti**, a combination of the elements or a combination of Cu with Sn or Zn. The invention also relates

to a method for producing such an adhesion-promoting layer. The inventive coating promotes the adhesion of pure metal layers which are applied to elec. insulating base materials of **microelectronics**, such as **polyimide**. The inventive coating achieves adhesion values of far >8 N/cm required in **microelectronics**.

RE.CNT 7 THERE ARE 7 CITED REFERENCES AVAILABLE FOR THIS RECORD
ALL CITATIONS AVAILABLE IN THE RE FORMAT

L18 ANSWER 15 OF 48 HCAPLUS COPYRIGHT 2002 ACS
AN 2000:483219 HCAPLUS
DN 133:216377
TI Sputtered coatings for microfluidic applications
AU Matson, Dean W.; Martin, Peter M.; Bennett, Wendy D.; Johnston, John W.; Stewart, Donald C.; Bonham, Charles C.
CS Pacific Northwest National Laboratory, Richland, WA, 99352, USA
SO Journal of Vacuum Science & Technology, A: Vacuum, Surfaces, and Films (2000), 18(4, Pt. 2), 1998-2002
CODEN: JVTAD6; ISSN: 0734-2101
PB American Institute of Physics
DT Journal
LA English
AB Magnetron sputter-deposited features and coatings are finding a broad range of uses in microfluidic devices being developed at the Pacific Northwest National Lab. Such features are routinely incorporated into multilayer laminated microfluidic components where specific functionality is required, and where other methods for producing these features have been deemed unacceptable. Applications include electrochem. sensors, heaters and temp. probes, elec. leads and insulation layers, piezoelec. actuators and transducers, and chem. modification of surfaces. Small features, such as those required for the prodn. of microsensor electrodes or miniature resistive heaters on microfluidic **chips**, were patterned using std. lithog. methods, or with masks produced by **laser** micromachining processes. Thin-film piezoelec. materials such as aluminum nitride have been deposited at low temps. for use with temp. sensitive materials. Use of the coating technol. and its application in the fabrication of specific microfluidic devices, including a groundwater sensor, miniature piezoelec. ultrasonic transducers and actuators, a polymerase chain reaction thermal cycler, and a microchannel flow diagnostic device, are discussed. Tech. issues assocd. with these coatings, such as adhesion, chem. resistance, and surface defects are also addressed.

RE.CNT 12 THERE ARE 12 CITED REFERENCES AVAILABLE FOR THIS RECORD
ALL CITATIONS AVAILABLE IN THE RE FORMAT

L18 ANSWER 16 OF 48 HCAPLUS COPYRIGHT 2002 ACS DUPLICATE 1
AN 2000:857806 HCAPLUS
DN 134:124201
TI Thermal management using planarized CVD-diamond substrates
AU Singh, Sushila B.; Krishnamoorthy, Arun; Malshe, Ajay P.; Naseem, Hameed; Brown, W. D.
CS High Density Electronics Center (HiDEC) Department of Mechanical Engineering, University of Arkansas, Fayetteville, AR, 72701-1201, USA
SO International Journal of Microcircuits and Electronic Packaging (2000), 23(1), 99-109
CODEN: IMEPE5; ISSN: 1063-1674
PB IMAPS - International Microelectronics and Packaging Society
DT Journal

LA English
AB CVD diamond (CVDD) substrates offer an outstanding soln. for various advanced electronic packaging applications such as high power 3-dimensional MCMs **laser** diodes, and high power MOSFETs. In the manufg. of such substrates, various post-synthesis processing steps, such as polishing, cutting, and metalization, add significantly to the cost of the package. Recently, the authors introduced a planarization-by-filling process to reduce the cost of polishing and increase the ease of manufg. The process involves surface planarization of coarsely-lapped diamond substrates using a filler material such as **polyimide**, which is regularly used in electronic packaging industry. In the past, the researchers demonstrated successfully the applicability of this planarization process. The authors present Finite Element anal. (FEA) and exptl. results of thermal management using **polyimide** planarized CVDD substrates, for wirebond and Flip **Chip die** attachment configurations. Specifically, these results are directed at detg. the max. **die** temp. for various power densities using liq. convection for edge cooling. Also, the paper presents results of a thermal stress study, using thermal shock, for GaAs **laser** diodes mounted, using gold-**tin** hard solder, on a CVDD substrate planarized using P1-2610 and 2611 **polyimides**. The planarization-by-filling process not only gives an easy and inexpensive soln. to the high surface roughness of CVDD, but also adds value to the package by providing a compliant layer between the GaAs **die** and CVDD without sacrificing thermal management performance.
RE.CNT 21 THERE ARE 21 CITED REFERENCES AVAILABLE FOR THIS RECORD
ALL CITATIONS AVAILABLE IN THE RE FORMAT

L18 ANSWER 17 OF 48 HCAPLUS COPYRIGHT 2002 ACS
AN 2000:902101 HCAPLUS
DN 134:201388
TI Thin film NiTi shape memory alloy microactuator with two-way effect
AU Gill, John J.; Carman, Gregory P.
CS Mechanical Aerospace Engineering Department, University of California, Los Angeles, CA, 90095-1597, USA
SO Micro-Electro-Mechanical Systems (2000), 2, 89-95
CODEN: MSIYAW
PB American Society of Mechanical Engineers
DT Journal
LA English
AB Thin film SMA (Shape memory alloy) is a useful material for MEMS (Microelectromech. Systems) actuator. This is because the thin film has an improved frequency response compared to bulk SMA, high work d., and produces large strain. A novel two-way thin film Ni-**Ti** shape memory alloy actuator is presented. Thin film shape memory alloy is sputter-deposited onto a Si **wafer** in an ultra-high vacuum system. Transformation temps. of the Ni-**Ti** film are detd. by measuring the residual stress as a function of temp. Test results show that the Martensite-Temp.-Finish (Mf) is .apprx.60.degree., and the Austenite-Temp.-Finish (Af) is 110.degree.. A free standing Ni-**Ti** membrane (12 mm .times. 12 mm and 2.5 .mu.m thick) is fabricated using MEMS technol. A mixt. of HF, HNO3 and DI (Deionized) H2O with thick photoresist mask works best for the fabrication process. The membrane is hot-shaped into a dome shape. When the temp. of the Ni-**Ti** film exceeds Af, the NiTi membrane transforms into the trained hot-shape. When the temp. cools down to room temp., the membrane returns to the initial flat shape. The performance of the SMA micro actuator was characterized

with a **laser** measurement system for deflection vs. input power and frequency response. The max. deflection of SMA microactuator is 230 .mu.m. The corresponding frequency responses at the max. deflection are 30 Hz with Cu block placed underneath the microactuator and <1 Hz when Plexiglass is placed.

RE.CNT 18 THERE ARE 18 CITED REFERENCES AVAILABLE FOR THIS RECORD
ALL CITATIONS AVAILABLE IN THE RE FORMAT

L18 ANSWER 18 OF 48 INSPEC COPYRIGHT 2002 IEE
AN 2001:7042502 INSPEC DN B2001-10-2220J-003
TI Sol-gel-derived 0-3 composite materials for direct-write electronics applications.
AU Coleman, S.M. (Dept. of Chem., Oklahoma State Univ., Stillwater, OK, USA); Parkhill, R.L.; Taylor, R.M.; Knobbe, E.T.
SO Materials Development for Direct Write Technologies. Symposium (Materials Research Society Symposium Proceedings Vol.624)
Editor(s): Chrisey, D.B.; Gamota, D.R.; Helvajian, H.; Taylor, D.P.
Warrendale, PA, USA: Mater. Res. Soc, 2000. p.53-8 of xiv+283 pp. 4 refs.
Conference: San Francisco, CA, USA, 24-26 April 2000
ISBN: 1-55899-532-3
DT Conference Article
TC Application; Practical; Experimental
CY United States
LA English
AB The use of sol-gel-derived 0-3 composite ceramics for low-temperature direct-write electronics applications was investigated. The 0-3 composite paste materials were prepared using selected metal alkoxides and commercial low- and high- kappa ' dielectric powders. The composite pastes were deposited on alumina and **polyimide** substrates using conventional screening and micro-dispensing techniques. The deposited films were oven-dried at or below 200 degrees C and thermally densified using a CO2 **laser**. The 0-3 composites exhibited good adhesion and structural density. Electrical characterization of the **laser** -processed dielectrics revealed kappa ' values as high as 295 and **tan** delta as low as 0.02 on **polyimide** substrates.

L18 ANSWER 19 OF 48 HCAPLUS COPYRIGHT 2002 ACS
AN 2000:229975 HCAPLUS
DN 133:35875
TI Photonic switch and NOT logic gate based on the hybrid integration of a GaAs VCSEL and a GaAs MISS
AU Kang, Xuejun; Lin, Shiming; Liao, Qiwei; Cheng, Peng; Gao, Junhua; Liu, Shi'an; Wang, Hongjie; Zhang, Chunhui; Wang, Qiming; Du, Guotong; Liu, Ying; Li, Xuemei
CS State Key Laboratory on Integrated Optoelectronics, Institute of Semiconductors, Chinese Academy of Sciences, Beijing, 100083, Peop. Rep. China
SO Chinese Journal of Electronics (2000), 9(1), 21-24
CODEN: CHJEEW; ISSN: 1022-4653
PB Chinese Institute of Electronics
DT Journal
LA English
AB The hybrid integrated photonic switch and not logic gate based on the integration of a GaAs VCSEL (Vertical Cavity Surface Emitting **Lasers**) and a MISS (Metal-Insulator-Semiconductor Switches) device are reported. The GaAs VCSEL is fabricated by selective etching and selective oxidn. The Ultra-Thin semi-Insulating layer (UTI) of the GaAs

MISS is formed by using oxidn. of AlAs that is grown by MBE. The accurate control of UTI and the processing compatibility between VCSEL and MISS are solved by this procedure. If a VCSEL is connected in series with a MISS, the integrated device can be used as a photonic switch, or a light amplifier. A low switching power (10.mu.W) and a good on-off ratio (17 dB contrast) were achieved. If they are connected in parallel, they perform a photonic NOT gate operation.

RE.CNT 8 THERE ARE 8 CITED REFERENCES AVAILABLE FOR THIS RECORD
ALL CITATIONS AVAILABLE IN THE RE FORMAT

L18 ANSWER 20 OF 48 HCAPLUS COPYRIGHT 2002 ACS
AN 1999:231471 HCAPLUS
DN 130:273895
TI Nitride semiconductor device
IN Toyota, Tatsunori; Takaoka, Yoshikazu
PA Nichia Chemical Industries Co., Ltd., Japan
SO Jpn. Kokai Tokkyo Koho, 7 pp.
CODEN: JKXXAF
DT Patent
LA Japanese
FAN.CNT 1

PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
JP 11097742	A2	19990409	JP 1997-256317	19970922

AB The invention relates to a nitride semiconductor device that is mounted on a lead frame by a flip-**chip** bonding technique, wherein the 1-10 .mu. thick **polyimide** film is fabricated on the insulating film of the device, so that the damages on the nitride semiconductor layer and the insulating film, due to the push-pin used for removing the device from the sticking tape in the prodn. process, may be avoided.

L18 ANSWER 21 OF 48 INSPEC COPYRIGHT 2002 IEE
AN 2000:6736805 INSPEC DN B2000-12-0170J-025
TI Thermal management using planarized CVD-diamond substrates.
AU Singh, S. (Dept. of Mech. Eng., Arkansas Univ., Fayetteville, AR, USA); Krishnamoorthy, A.; Malshe, A.P.; Naseem, H.A.; Brown, W.D.
SO Proceedings of the SPIE - The International Society for Optical Engineering (1999) vol.3906, p.745-51. 6 refs.
Published by: SPIE-Int. Soc. Opt. Eng
CODEN: PSISDG ISSN: 0277-786X
SICI: 0277-786X(1999)3906L.745:TMUP;1-1
Conference: 1999 International Symposium on Microelectronics. Chicago, IL, USA, 26-28 Oct 1999
Sponsor(s): IMAPS
DT Conference Article; Journal
TC Theoretical; Experimental
CY United States
LA English
AB CVD diamond (CVDD) substrates offer an outstanding solution for various advanced electronic packaging applications such as high power 3-D MCMS, **laser** diodes, and high power MOSFETs. In the manufacturing of such substrates, various post-synthesis processing steps, such as polishing, cutting, and metallization, add significantly to the cost of the package. Recently, we introduced a planarization-by-filling process to reduce the cost of polishing and increase the ease of manufacturing. The process involves surface planarization of coarsely-lapped diamond substrates using a filler material such as **polyimide**. In the past, we

demonstrated successfully the applicability of this planarization process. In this paper, we present results of a parametric thermal management study on such substrates under various ambient conditions. Specifically, the results of experimental work and finite element analysis (FEA) directed at determining maximum **die** temperature for various power densities using liquid convection for edge cooling are presented. Also, the paper presents results of a thermal stress study, using thermal shock, for GaAs **laser** diodes mounted, using gold-**tin** solder, on a diamond substrate planarized using PI-2610 and 2611 **polyimides**.

L18 ANSWER 22 OF 48 INSPEC COPYRIGHT 2002 IEE
AN 2001:6858116 INSPEC DN B2001-04-2210D-054
TI New excimer **laser** technology-ultra fine lines (15 mu m) without etching.
AU Kickelhain, J. (LPKF Laser & Electron. AG, Garbsen, Germany)
SO Proceedings. Electronic Circuits World Convention 8
Birmingham, UK: Electronics Circuits World Convention 8, 1999. p.PO1ka-c of CD-ROM pp. 0 refs.
Conference: Tokyo, Japan, 7-10 Sept 1999
Sponsor(s): Japan Printed Circuit Assoc.; Eur. Inst. of Printed Circuits; Assoc. Connecting Electron. Ind
DT Conference Article
TC Practical
CY United Kingdom
LA English
AB The miniaturization of electronic components requires the development of new materials and technologies for reduction of lines and spaces in PCBs. An excimer **laser** system (248 nm) working in projection mode was developed for the structuring of ultra fine lines without etching techniques. Layout dimensions of 100*100 mm with a total processing range of 200*200 mm and a processing speed of 10 cm2/s allow a high-volume production process. A fully-additive metallization process with copper, nickel, gold or **tin**/lead reveals numerous applications in the electronics industry, e.g. flexible interposers (CSP), microcoils and other micro-structures for interconnections. The base material is an adhesiveless flexible polymer foil, e.g. **polyimide**, with a plating base consisting of **laser** structured gold or copper. This excimer **laser** technology also enables the micro-structuring of thin polymer layers, e.g. dielectric layers.

L18 ANSWER 23 OF 48 HCAPLUS COPYRIGHT 2002 ACS
AN 1998:394266 HCAPLUS
DN 129:38350
TI Laminated assembly for active bioelectronic devices
IN Ackley, Donald E.; Jackson, Thomas R.; Sheldon, Edward L., III
PA Nanogen, Inc., USA
SO PCT Int. Appl., 35 pp.
CODEN: PIXXD2
DT Patent
LA English
FAN.CNT 37

PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI WO 9824544	A1	19980611	WO 1997-US21898	19971126
W: AU, BR, CA, CN, JP, KR				
RW: AT, BE, CH, DE, DK, ES, FI, FR, GB, GR, IE, IT, LU, MC, NL, PT, SE				
US 6287517	B1	20010911	US 1996-753962	19961204

	AU 9853671	A1	19980629	AU 1998-53671	19971126
	AU 733523	B2	20010517		
	EP 961652	A1	19991208	EP 1997-950750	19971126
	R: AT, BE, CH, DE, DK, ES, FR, GB, GR, IT, LI, LU, NL, SE, MC, PT, IE, FI				
	BR 9713991	A	20000208	BR 1997-13991	19971126
	JP 2002501611	T2	20020115	JP 1998-525705	19971126
PRAI	US 1996-753962	A	19961204		
	US 1993-146504	A2	19931101		
	US 1994-271882	A2	19940707		
	US 1994-304657	A2	19940909		
	US 1995-534454	A2	19950927		
	US 1996-709358	A2	19960906		
	WO 1997-US21898	W	19971126		

AB Methods of manuf. and devices for performing active biol. operations utilize laminated structures. In the preferred embodiment, a first planar sample support includes at least one sample through hole a planar electrode is disposed adjacent the first planar sample support, and includes an electrode through region, a second planar support includes a vent through hole, the planar electrode being in a laminated relationship between the first planar sample support and the second planar support, further characterized in that the sample through hole, electrode through hole and vent through hole are in overlapping arrangement. Preferably, some or all of the through holes, through regions and vent through holes are aligned. In one embodiment, the lateral dimension of the vent through hole is larger than the lateral dimension of the electrode through hole. In an alternative embodiment, the lateral dimension of the sample through hole is larger than the lateral dimension of the vent through hole. In the preferred embodiment, the sample support and planar support are formed of sheet material, most preferably **polyimide**, having a thickness from substantially 1 to substantially 5 mils. Electrodes are preferably chosen from noble metals, esp. gold. Holes or through regions are preferably formed through **laser** drilling, optionally followed by chem. etching. Interconnect vias provide conductive paths through multiple supports, and are advantageously utilized with hybridized circuitry, esp. **chip**-on flex circuitry.

L18 ANSWER 24 OF 48 INSPEC COPYRIGHT 2002 IEE
AN 1999:6327574 INSPEC DN B1999-10-0170J-003
TI Conductive polymers for **microelectronic** packaging: **chip** bonding to polymer films.
AU Kuchenmeister, F.; Bottcher, M.; Meusel, E. (Semicond. & Microsyst. Technol. Lab., Tech. Univ. Dresden, Germany); Meier, D.
SO Polymers for Advanced Technologies (Oct.-Nov. 1998) vol.9, no.10-11, p.806-11. 10 refs.
Published by: Wiley
Price: CCCC 1042-7147/98/100806-06$17.50
CODEN: PADTE5 ISSN: 1042-7147
SICI: 1042-7147(199810/11)9:10/11L.806:CPMP;1-0
Conference: Fourth International Symposium on Polymers for Advanced Technologies (PAT'97). Leipzig, Germany, 31 Aug-4 Sept 1997
Sponsor(s): Polymers for Adv. Technol
DT Conference Article; Journal
TC Experimental
CY United Kingdom
LA English
AB A novel flipchip-like **microelectronic** packaging technology for

bonding **integrated circuits** to polymer foils using a **laser** micromachining technique and a wet chemical metallization process of conductive polymers has been developed. This paper will focus on the deposition of polypyrrole onto the aluminum surface and the characterization of the thin film using scanning electron microscopy, Auger electron spectroscopy and X-ray photoelectron spectroscopy. The conductive polymer is metallized by copper electroplating for connecting the **integrated circuit** to the **polyimide** foil. Electrical measurements were performed on patterned substrates with a layer system consisting of polypyrrole/copper/**tin**-lead deposited on aluminum bond pads. The characteristic current/voltage curve shows an ohmic contact behavior which is of fundamental importance for the development of **chip** bonding technology using conductive polymers.

L18 ANSWER 25 OF 48 HCAPLUS COPYRIGHT 2002 ACS
AN 1999:383368 HCAPLUS
DN 131:185838
TI Pulsed **laser** deposition of **TiN** on PMMA and **polyimide**: a novel route for polymer metallization
AU Vispute, R. D.; Narayan, J.; Jagannadham, K.
CS Department of Materials Science and Engineering, North Carolina State University, Raleigh, NC, 27695, USA
SO Metallized Plastics 5 & 6: Fundamental and Applied Aspects, [Proceedings of the Symposia], 5th and 6th, Los Angeles and Paris, 1996, 1997 (1998), Meeting Date 1996-1997, 25-39. Editor(s): Mittal, Kashmiri Lal. Publisher: VSP, Utrecht, Neth.
CODEN: 67SWA9
DT Conference
LA English
AB A method for metalization of polymeric materials is based on pulsed **laser** deposition. Highly metallic, adherent and hard **TiN** films were deposited using KrF excimer **laser** ablation of high purity, stoichiometric and hot pressed **TiN** target at a base pressure of 1x10-7 Torr, and the ablated species were allowed to condense on the polymeric substrate materials. The **laser** fluence, pulse repetition rate, substrate-to-target distance, and substrate temp. were optimized for fabrication of high quality metallic and adherent **TiN** films on PMMA and **polyimide**. The films were characterized by Auger electron spectroscopy, Raman spectroscopy, scanning and transmission electron microscopies, and four-point-probe elec. resistivity. Auger spectroscopy revealed that the films were close to stoichiometric **TiN**. The **TiN** films deposited on **polyimide** and PMMA were smooth, golden in color, and were polycryst. with an av. grain size of about 12 nm. The adhesion of **TiN** films was measured by the direct pull-off method. The films were highly adherent to the polymer substrates as compared to Cu and Au films deposited by sputtering. Four-point-probe elec. resistivity measurements showed characteristic metallic behavior with a low value of resistivity, 30-75 .mu..OMEGA.-cm, at room temp. The specific resistivity was a strong function of deposition temp. and reached the lowest value of 15 .mu..OMEGA.-cm at room temp. for epitaxial **TiN** films on Si (100) deposited at 600.degree. by pulsed **laser** deposition. **Laser** etching of **TiN** films on polymers leads to insulator/metal/polymer multilayer structures (AlN/**TiN**/polymer, diamond-like carbon (DLC)/**TiN**/polymer) for multi-**chip** modules in electronics packaging applications.

RE.CNT 25 THERE ARE 25 CITED REFERENCES AVAILABLE FOR THIS RECORD
ALL CITATIONS AVAILABLE IN THE RE FORMAT

L18 ANSWER 26 OF 48 HCAPLUS COPYRIGHT 2002 ACS DUPLICATE 2
AN 1997:87104 HCAPLUS
DN 126:205329
TI "All-dry" and in situ microstructuring of carbide/**polyimide** layers
AU Danev, G.; Spassova, E.; Patkov, K.; Assa, J.; Ihleman, J.; Wolf-Rottke, B.
CS Central Laboratory of Photoprocesses, Bulgarian Academy of Sciences, Sofia, 1113, Bulg.
SO Vacuum (1997), 48(1), 63-67
CODEN: VACUAV; ISSN: 0042-207X
PB Elsevier
DT Journal
LA English
AB The capacities of a new "all-dry" resist system for in situ microstructuring have been investigated. The system consists of a 1000 nm thick vacuum deposited polymer (**polyimide**) layer and a 40 nm thick electron-beam evapd. carbide (TiC or B4C) film. The bilayer system is patterned in situ in two stages. The microstructuring of the carbide film is carried out by a single pulse excimer **laser** exposure at threshold fluences of 27 mJ/cm2 and 23 mJ/cm2 for TiC and B4C, resp. The **laser** generated image is transferred into the bottom **polyimide** layer by reactive ion etching in an O2 ambience. The proposed all-dry lithog. system provides an attractive scientific and technol. basis for the integrated microstructuring processes, easily adaptable to the existing **microelectronic** technologies.

L18 ANSWER 27 OF 48 INSPEC COPYRIGHT 2002 IEE
AN 1998:6015996 INSPEC DN B9810-4270-029
TI Hybrid integration of smart pixel with vertical-cavity surface-emitting **laser** using **polyimide** bonding.
AU Matsuo, S. (NTT Network Service Syst. Labs., Tokyo, Japan); Nakahara, T.; Tateno, K.; Tsuda, H.; Kurokawa, T.
SO Spatial Light Modulators. Topical Meeting. OSA Trends in Optics and Photonics Series. Vol.14
Editor(s): Burdge, G.; Esener, S.C.
Washington, DC, USA: Opt. Soc. America, 1997. p.39-46 of ix+284 pp. 11 refs.
Conference: Incline Village, NV, USA, 17-19 March 1997
Sponsor(s): Opt. Soc. America
ISBN: 1-55752-487-4
DT Conference Article
TC Practical; Experimental
CY United States
LA English
AB We have developed a new three-dimensional integration technology which involves hybrid integration of photonic and electronic circuits by means of **polyimide** bonding. To demonstrate this technology, a vertical-cavity surface-emitting **laser** (VCSEL) and metal-semiconductor-metal photodetector arrays were fabricated on a Si substrate. The photoresponsivity of the photodetector was 0.3 A/W . The threshold current of the VCSEL was 3.1 mA and the maximum output power was 2.45 mW for a 15- mu m-diameter mesa at 20 degrees C. The VCSEL was not lasing above 90 degrees C. The calculation shows the thermal

resistance for the proposed hybrid structure strongly depends on the **polyimide** thickness. The difference in active layer temperature between the hybrid and monolithic structures is within 10 K when the thickness of the **polyimide** is less than 0.1 mu m and the electrical power consumption is 30 mW. We also calculated the power consumption and the maximum number of pixels per **chip**. A lower threshold current of the VCSELs and a lower bias voltage to the Si-CMOS circuit are desired to obtain a higher I/O throughput device.

L18 ANSWER 28 OF 48 HCAPLUS COPYRIGHT 2002 ACS
AN 1996:397339 HCAPLUS
DN 125:73689
TI **Laser** method for plating vias
IN Owen, Mark D.
PA Electro Scientific Industries, Inc., USA
SO PCT Int. Appl., 40 pp.
CODEN: PIXXD2
DT Patent
LA English
FAN.CNT 1

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	WO 9612830	A1	19960502	WO 1995-US8474	19950706
	W: CH, DE, JP, KR, SG				
	RW: AT, BE, CH, DE, DK, ES, FR, GB, GR, IE, IT, LU, MC, NL, PT, SE				
	DE 19581659	T	19970522	DE 1995-19581659	19950706
	EP 787219	A1	19970806	EP 1995-926182	19950706
	EP 787219	B1	19981111		
	R: CH, DE, GB, LI				
	CH 688415	A	19970915	CH 1996-3109	19950706
	JP 09511791	T2	19971125	JP 1995-513873	19950706
	JP 2948915	B2	19990913		
PRAI	US 1994-327484		19941020		
	WO 1995-US8474		19950706		

AB The output of a continuously pumped, Q-switched, Nd:YAG **laser** is frequency converted to provide UV light for plating internal wall surfaces of vias in multilayer electronic devices. The parameters of the output pulses are selected to facilitate substantially uniform deposition of plating material particles explosively vaporized from a substrate onto the internal wall surface. These parameters typically include .gtoreq.2 of the following criteria: high av. power of .gtorsim.100 mW measured over the beam spot area, a temporal pulse width shorter than .apprx.100 ns, a spot diam. of .ltorsim.50 .mu.m, and a repetition rate of .gtorsim.1 kHz.

L18 ANSWER 29 OF 48 INSPEC COPYRIGHT 2002 IEE
AN 1996:5446577 INSPEC DN B9701-2550F-034
TI Direct writing of gold and copper lines from solutions.
AU Wehner, M.; Legewie, F.; Theisen, B.; Beyer, E. (Fraunhofer-Inst. fur Lasertechnik, Aachen, Germany)
SO Applied Surface Science (Oct. 1996) vol.106, p.406-11. 10 refs.
Doc. No.: S0169-4332(96)00388-1
Published by: Elsevier
Price: CCCC 0169-4332/96/$15.00
CODEN: ASUSEE ISSN: 0169-4332
SICI: 0169-4332(199610)106L.406:DWGC;1-I
Conference: Second International Conference on Photo-Excited Processes and Applications. Jerusalem, Israel, 17-21 Sept 1995

Sponsor(s): Center for Tech. Educ. Holon; Tel-Aviv Univ.; Hebrew Univ.; et al
DT Conference Article; Journal
TC Practical
CY Netherlands
LA English
AB For printed circuit repair and fine pitch wiring a metallization technique is investigated which could be applied in ambient air. Organo-metallic precursors containing gold or copper are dissolved in a variety of solvents and spilled onto the substrate. Dimethylenglykoldimethylether, DME, exhibits best properties with respect to a high solubility of the precursor and slow evaporation of the solvent. With second harmonic Nd:YAG or argon ion **laser** radiation of 150 mW power metal lines are written on **polyimide** from organo-gold(I) and copper compounds with a writing speed of 0.6 mm/s. First results of writing on SiC substrates with Nd:YAG **laser** radiation of 3 **W** power from PEt3AuCl are reported. Micrographs and measurements of the resistivity of the **laser** written lines are given.

L18 ANSWER 30 OF 48 INSPEC COPYRIGHT 2002 IEE
AN 1997:5590822 INSPEC DN B9707-2250-003
TI Embedded thin film resistors, capacitors, and inductors in flexible **polyimide** films.
AU Lenihan, T.; Schaper, L.; Shi, Y.; Morcan, G.; Fairchild, K. (High Density Electron. Center, Arkansas Univ., Fayetteville, AR, USA)
SO Proceedings of the 1996 International Electronics Packaging Conference Edina, MN, USA: Int. Electron. Packaging Soc, 1996. p.192-202 of 681 pp. 17 refs.
Conference: Austin, TX, USA, 29 Sept-1 Oct 1996
Sponsor(s): Int. Electron. Packaging Soc
DT Conference Article
TC Application; Practical; Experimental
CY United States
LA English
AB Embedding thin film passive devices into **polyimide** layers as part of an MCM allows separate fabrication and test of embedded passive devices before assembling them into an MCM-L substrate, providing a low cost alternative to current MCM-L and MCM-D technologies. The embedded devices can be made into a flexible MCM package using the interconnected mesh power system (IMPS) two layer interconnect system. The IMPS topology uses fine line lithography and batch via generation for planar power and ground distribution and dense signal interconnection on two metal layers. The materials under test are NiCr, **TaN**, and CrSi for resistors, and BaTiXOY and TaXOY for capacitors. Using proven passive device materials such as CrSi and TaXOY minimizes development time. Cu metallurgy is used for contacts, signal lines, and power lines. The devices are made on 50 mu m thick **polyimide** film and encapsulated with **polyimide**. Contact openings are made using a **laser** or lithography and device films are stacked on IMPS redistribution layers. **Chips** are then mounted on the surface and encapsulated, completing the integrated package. Test vehicles were designed using standard value passive devices with characterization, tuned circuit, and reliability structures. Devices were evaluated at high frequencies and effects due to capacitive coupling within devices and with external materials were modelled. Preliminary results of thermal shock and mechanical flexing reliability tests are encouraging. Potential applications for this type of MCM are discussed. The films can be combined with thermal heat spreaders

and heat sinks.

L18 ANSWER 31 OF 48 INSPEC COPYRIGHT 2002 IEE
AN 1997:5519801 INSPEC DN B9704-4270-012
TI VCSEL-based smart pixels.
AU Matsuo, S.; Kurokawa, T. (NTT Opto-Electron. Labs., Kanagawa, Japan)
SO Digest. IEEE/LEOS 1996 Summer Topical Meetings. Advanced Applications of Lasers in Materials Processing; Broadband Optical Networks - Enabling Technologies and Applications; Smart Pixels; Optical MEMs and their Applications (Cat. No.96TH8164)
New York, NY, USA: IEEE, 1996. p.3-4 of vi+78 pp. 7 refs.
Conference: Keystone, CO, USA, 5-9 Aug 1996
Sponsor(s): Eng. Found
ISBN: 0-7803-3175-3
DT Conference Article
TC General Review; Practical
CY United States
LA English
AB Smart pixels incorporating vertical-cavity surface-emitting **lasers** (VCSELs) have shown great potential for use in optical computing systems and photonic switching networks because the integration of the VCSEL makes optical circuits easy to construct. We have developed integration with a VCSEL, MESFETs, and a metal-semiconductor-metal (MSM) photodetector. In this device, both NOR- and OR-types of operation can be performed with the same circuit. The device operated at a high contrast ratio of more than 30 dB with optical gain. It also showed the 3-dB bandwidth of 220 MHz with 300- mu **W** input power. We recently proposed a novel structure that uses three-dimensional integration of the compound semiconductor thin-film and a silicon circuit. The VCSEL and photodetector layers are bonded onto a silicon circuit using **polyimide**. This method does not require any alignment before **wafer** bonding. The fabrication process for the photonic circuit is the same technology that is used in our monolithic integrated smart pixel, so it facilitates a **wafer** -scale fabrication process. To demonstrate this technology, we fabricated an MSM photodetector on a silicon substrate.

L18 ANSWER 32 OF 48 HCAPLUS COPYRIGHT 2002 ACS
AN 1995:965024 HCAPLUS
DN 124:43268
TI Thin-film circuits with high-density connectors
IN Castleberry, Donald E.
PA General Electric Company, USA
SO U.S., 6 pp.
CODEN: USXXAM
DT Patent
LA English
FAN.CNT 1

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	US 5463242	A	19951031	US 1994-237702	19940503
	US 5489551	A	19960206	US 1995-376209	19950120
PRAI	US 1994-237702		19940503		

AB A method of fabricating a high-d. thin-film circuit includes bonding a high-d. connector having a plurality of elec. connection lines with a **wafer** having a plurality of elec. contact pads arranged in a pattern with a pitch .ltorsim.100 .mu.m so that elec. couplings are formed between resp. **wafer** contact pads and corresponding connection

lines. The step of forming the elec. coupling comprises pyrolysis of an adhesive disposed between the high-d. connector and the **wafer**. The elec. couplings between resp. contact pads and corresponding connection lines are formed by directing a **laser** beam on the area in which an elec. coupling is to be formed, to cause thermal decompn. of the adhesive to form a conductive C material; portions of the **wafer** contact pad and the connection line are also welded to the conductive C material due to heating by the pulsed **laser**.

L18 ANSWER 33 OF 48 HCAPLUS COPYRIGHT 2002 ACS
AN 1995:420272 HCAPLUS
DN 122:162916
TI Solid surface modifying process and apparatus
IN Murahara, Masataka; Urairi, Masakatsu
PA Tokai University, Japan; Nitto Denko Corp.
SO PCT Int. Appl., 74 pp.
CODEN: PIXXD2
DT Patent
LA Japanese
FAN.CNT 1

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	WO 9421715	A1	19940929	WO 1994-JP463	19940323
	W: US				
	RW: DE, FR, GB, IT				
	JP 06293837	A2	19941021	JP 1993-80435	19930407
	JP 06329818	A2	19941129	JP 1993-238350	19930924
	JP 06335631	A2	19941206	JP 1993-238349	19930924
	JP 06340759	A2	19941213	JP 1993-238351	19930924
	EP 644227	A1	19950322	EP 1994-910522	19940323
	R: DE, FR, GB, IT				
	US 6117497	A	20000912	US 1997-888862	19970707
PRAI	JP 1993-64096	A	19930323		
	JP 1993-76888	A	19930402		
	JP 1993-80435	A	19930407		
	JP 1993-83555	A	19930409		
	JP 1993-238349	A	19930924		
	JP 1993-238350	A	19930924		
	JP 1993-238351	A	19930924		
	WO 1994-JP463	W	19940323		

AB The title process consists of keeping a surface of a solid material (e.g., synthetic resin, glass, a metal and a ceramic material) in contact with a liq. compd. or a compd. soln. (e.g., H2O, formic acid, aq. ammonium borate, etc.), applying radiation selected from UV, visible light, and/or IR to an interface between the solid material and the liq. compd. or compd. soln. in order to substitute or accumulate the chem. groups in the liq. compd. or compd. soln. on the surface, or etching the surface with the chem. groups. The treatment enables the irradiated portion to have good hydrophilic and adhesive property, printability, corrosion resistance, and elec. cond.

L18 ANSWER 34 OF 48 HCAPLUS COPYRIGHT 2002 ACS DUPLICATE 3
AN 1994:713153 HCAPLUS
DN 121:313153
TI Studies on the high-temperature superconductor (HTS)/metal/polymer dielectric interconnect structure for packaging applications
AU Paik, Kyung W.; Mogro-Campero, Antonio

CS General Electric Corporate Research and Development, Schenectady, NY, 12301, USA
SO IEEE Transactions on Components, Packaging, and Manufacturing Technology, Part B: Advanced Packaging (1994), 17(3), 435-41
CODEN: IMTBE4; ISSN: 1070-9894
DT Journal
LA English
AB A HTS/metal/low dielec. const. polymer dielec. hybrid interconnect structure was fabricated using high d. interconnect (HDI) Cu/**polyimide** processing techniques. Non-degraded superconducting properties, Jc of over 1 MA cm-2 and Tc of 88 K, were obtained using optimum processing conditions. A 0.6 .mu.m-thick YBCO film was co-evapd. on LaAlO3 substrate, annealed, patterned, and Au contact pads were deposited. A Kapton **polyimide** film was laminated on HTS parts in an O environment. using a siloxane **polyimide** (SPI) base adhesive at 170-210.degree. or a polyester base adhesive at 150.degree. Vias were drilled on the polymer layer using a 351. nm Ar **laser** followed by subsequent via cleaning with O2 + CF4 plasma. To complete test parts **Ti**/Cu/**Ti** metalization and patterning with a **laser** adaptive lithog. were followed. The laminated polymer film on the HTS protected HTS film properties from heating and H2O exposure. The **polyimide** laminated HTS film maintains its supercond. up to 210.degree. of lamination temp. The hybrid structure also showed excellent reliability performances: 6% Jc decrease at 150.degree./65 h thermal bake, 12% Jc decrease after 100 thermal cycles from -96 to 150.degree., and maintain supercond. in H2O immersion up to >10 h. Tc of samples remained always the same 88 K. Coplanar HTS lines, microstrip HTS/metal lines, and HTS power strip line structures were demonstrated on a 2-in-diam. HTS **wafer** coupon.

L18 ANSWER 35 OF 48 HCAPLUS COPYRIGHT 2002 ACS DUPLICATE 4
AN 1995:634901 HCAPLUS
DN 123:272509
TI Studies on the high temperature superconductor (HTS)/metal/polymer dielectric interconnect structure for packaging applications
AU Paik, Kyung W.; Mogro-Campero, Antonio
CS General Electric Corporate Research and Development, Schenectady, NY, 12301, USA
SO Proceedings - Electronic Components & Technology Conference (1994), 44th, 362-6
CODEN: PETCES
PB Institute of Electrical and Electronics Engineers
DT Journal
LA English
AB A HTS/metal/low dielec. const. polymer dielec. hybrid interconnect structure was fabricated using high d. interconnect (HDI) copper/**polyimide** processing techniques. Nondegraded superconducting properties, Jc of over 1 MAcm-2 and Tc of 88K, were obtained using optimum processing conditions. A 0.6 .mu.m-thick YBCO film was coevaporated on LaAlO3 substrate, annealed, patterned, and Au contact pads were deposited. A siloxane **polyimide** (SPI) base adhesive at 170 - 210 .degree.C or a polyester base adhesive at 150 .degree.C was laminated on HTS parts in an oxygen environment. Vias were drilled on the polymer layer using a 351 nm Ar **laser** followed by subsequent via cleaning with O2+CF4 plasma. To complete test parts **Ti**/Cu/**Ti** metalization and patterning with a **laser** adaptive lithog. were followed. The laminated polymer film on the HTS protected HTS film properties from

heating and water. The laminated HTS film maintains its supercond. up to 210 .degree.C of lamination temp. The hybrid structure also showed excellent reliability performances: 6% Jc decrease at 150 .degree.C/65 h thermal bake, 12% Jc decrease after 100 thermal cycles from -196 to 150 .degree.C, and maintain supercond. in water immersion up to more than 10 h. Tc of samples remained always the same 88K. Coplanar HTS lines, microstrip HTS/metal lines, and HTS power strip line structures were demonstrated on a 2-in.-diam. HTS **wafer** coupon.

L18 ANSWER 36 OF 48 INSPEC COPYRIGHT 2002 IEE
AN 1995:4881146 INSPEC DN A9505-8115J-004; B9503-0520F-040
TI Diode **laser**-assisted deposition of gold and copper from thin organometallic films.
AU Evoy, S.; Bernier, M.-H.; Izquierdo, R.; Pieri, F.; Meunier, M.; Sacher, E. (Dept. de Genie Phys., Ecole Polytech. de Montreal, Que., Canada)
SO Electronic Packaging Materials Science VII Symposium
Editor(s): Borgesen, P.; Jensen, K.F.; Pollak, R.A.
Pittsburgh, PA, USA: Mater. Res. Soc, 1994. p.91-6 of xiii+450 pp. 16 refs.
Conference: Boston, MA, USA, 29 Nov-3 Dec 1993
DT Conference Article
TC Practical; Experimental
CY United States
LA English
AB We have developed a simple, compact and economical diode **laser** -assisted process for the direct writing of gold and copper on **polyimide**. Gold precursor films were deposited by spin-coating a commercially available organometallic compound onto the substrate. The local pyrolysis of these films was induced by the focused beam of an AlGaAs diode **laser** array (Pmax=1W, lambda =796 nm). Direct writing was achieved in open air while moving the substrate at speeds up to 15 mm/s. Gold lines 13-17 mu m wide, approximately 0.1 mu m thick, and having a resistivity of 30 mu Omega cm, were obtained on **polyimide** with good reproducibility using writing speeds >10 mm/s. Following a simple annealing process, these gold lines successfully activated the electroless plating of copper. After 45 min of plating, 2 mu m thick Cu-Au conductors, having a resistivity of 8 mu Omega .cm, were deposited. A commercially available copper precursor was also studied for the direct deposition of copper.

L18 ANSWER 37 OF 48 HCAPLUS COPYRIGHT 2002 ACS DUPLICATE 5
AN 1993:505710 HCAPLUS
DN 119:105710
TI Characterization, set-up, and control of a manufacturing **laser** ablation tool and process
AU Wolbold, Gerhard E.; Tessler, Christopher L.; Tudryn, Dawn J.
CS East Fishkill Fac., Int. Bus. Mach. Corp., Hopewell Junction, NY, 12533, USA
SO Proc. SPIE-Int. Soc. Opt. Eng. (1993), 1835(Excimer Lasers: Applications, Beam Delivery Systems, and Laser Design), 62-9
CODEN: PSISDG; ISSN: 0277-786X
DT Journal
LA English
AB The ablation of **polyimide** with an excimer **laser** ablation tool in a manufg. line is described. The light source is a 150 W XeCl (308 nm) gas **laser**. Two methods of ablating via patterns with the **laser** tool are: full-**chip** and scan

modes.

L18 ANSWER 38 OF 48 HCAPLUS COPYRIGHT 2002 ACS DUPLICATE 6
AN 1991:217535 HCAPLUS
DN 114:217535
TI Repetitively pulsed xenon monochloride **laser** with the power of 600 **W** for technological applications
AU Borisov, V. M.; Vinokhodov, A. Yu.; Gerasimov, S. M.; Evstratov, E. V.; Kiryukhin, Yu. B.; Kuznetsov, S. G.; Stepanov, Yu. Yu.; Vizir, V. A.; Manylov, S. P.; et al.
CS Inst. At. Energ. im. Kurchatova, Moscow, s, USSR
SO Kvantovaya Elektron. (Moscow) (1991), 18(2), 183-5
CODEN: KVEKA3; ISSN: 0368-7147
DT Journal
LA Russian
AB Results are presented of development of a powerful excimer **laser** which can emit radiation at .lambda. = 308 nm with an av. power of .apprx.600 **W**. The **laser** power supply system is designed on the basis of 4 com. produced thyratrons and a magnetic switch. Results of producing a hole structure in **polyimide** deposited on Al are presented as an example of the use of this **laser**. This binary film is a flexible carrier used for manuf. of large-scale **integrated circuits**.

L18 ANSWER 39 OF 48 INSPEC COPYRIGHT 2002 IEE
AN 1991:3848538 INSPEC DN B91024023
TI **Laser** direct writing of copper on various thin-film substrate materials (hybrid interconnections).
AU Muller, H.G.; Buschick, K.; Schuler, S.; Paredes, A. (Forschungschwerpunkt Mikroperipherik, Tech. Univ., Berlin, Germany)
SO Applied Surface Science (Dec. 1990) vol.46, p.143-7. 9 refs.
Price: CCCC 0169-4332/90/$03.50
CODEN: ASUSEE ISSN: 0169-4332
Conference: Symposium E on Surface Processing and Laser Assisted Chemistry ofthe 1990 E-MRS Spring Conference. Strasbourg, France, 29 May-1 June 1990
DT Conference Article; Journal
TC Experimental
CY Netherlands
LA English
AB **Laser** direct writing of copper from dried-on copper formate films on Al2O3, AlN, **polyimide** and aluminium is described. Writing speeds of 1 to 50 mm/s, and a **laser** power of up to 2 **W** have been used. On **polyimide**, argon **laser** writing is the preferred method. It is shown that multichip module interconnections may be written successfully with this method.

L18 ANSWER 40 OF 48 HCAPLUS COPYRIGHT 2002 ACS
AN 1990:450956 HCAPLUS
DN 113:50956
TI Investigation of photoablation as a patterning technique for silicon based **integrated circuits**: **laser** ablation and physical damage threshold considerations
AU Singleton, D. L.; Paraskevopoulos, G.; Buckthought, A. D.; Irwin, R. S.; Jolly, G. S.; Emesh, I. T. Ali
CS Div. Chem., Natl. Res. Counc. Canada, Ottawa, ON, K1A 0R6, Can.
SO Proc. SPIE-Int. Soc. Opt. Eng. (1990), Volume Date 1989, 1186(Surf. Interface Anal. Microelectron. Mater. Process. Growth), 48-55

CODEN: PSISDG; ISSN: 0277-786X
DT Journal
LA English
AB Damage threshold energies for a pulsed XeCl excimer **laser** at 308 nm were obtained for a no. of **microelectronic** materials which may have patterning applications. A photoacoustic technique is used to identify the damage process. An example of **laser** patterning illustrating the constraints on **laser** energy is given.

L18 ANSWER 41 OF 48 INSPEC COPYRIGHT 2002 IEE
AN 1990:3670203 INSPEC DN A90097692; B90048586
TI Surface and Interface Analysis of **Microelectronic** Materials Processing and Growth.
SO Proceedings of the SPIE - The International Society for Optical Engineering (1990) vol.1186
CODEN: PSISDG ISSN: 0277-786X
Conference: Surface and Interface Analysis of Microelectronic Materials Processing and Growth. Santa Clara, CA, USA, 12-13 Oct 1989
Sponsor(s): SPIE
DT Conference Proceedings; Journal
CY United States
LA English
AB The following topics were dealt with: optical characterisation of **microelectronic** processing by growing-incidence X-ray diffraction, X-ray fluorescence, contactless photoreflectance and **laser** oblation; optical characterisation of **microelectronic** growth of superconducting and semiconducting thin films including Raman microprobe MOLE, reflectance-difference spectroscopy, phase-modulated ellipsometry and photoreflectance; electron and ion microscopy of growth and processing of semiconductors, Al-SiO2, **W**, Cu-**polyimide** and LiNbO3 waveguides.

L18 ANSWER 42 OF 48 HCAPLUS COPYRIGHT 2002 ACS DUPLICATE 7
AN 1990:88045 HCAPLUS
DN 112:88045
TI Thermal and mechanical model of x-ray lithography masks under short pulse irradiation
AU Shareef, Iqbal; Maldonado, Juan R.; Katcoff, David
CS Gen. Technol. Div., IBM, Hopewell Junction, NY, 10533, USA
SO J. Vac. Sci. Technol., B (1989), 7(6), 1575-82
CODEN: JVTBD9; ISSN: 0734-211X
DT Journal
LA English
AB Computer simulations are presented of x-ray mask heating by fast x-ray pulses. Temp. distributions were obtained in an x-ray mask during exposure to x-ray pulses generated by a hot plasma. Three mask structures were studied: (1) Si-Au absorber, (2) Si-**polyimide**-Au absorber, and (3) Si-**W** absorber. The transient thermal anal. results were obtained using finite element modeling techniques (CAEDS and NASTRAN). The x-ray exposure was assumed to have taken place in a He atm. with a 40-.mu. gap between the mask and the **wafer**, which was assumed to be a heat sink at const. temp. The temp. distributions obtained above were subsequently used as input to study possible mech. deformation of the membrane. Again, finite element techniques were used and solns. were obtained by static stress methods. Results indicate a max. temp. rise on the mask of the order of 18.degree. for a 20-ns exposure by a 10 mJ/cm2 x-ray pulse. The max. termp. was obtained at the end of the x-ray pulse.

The temp. decayed quickly, reaching initial ambient temp. after .apprx.10 ms. Mech. anal. showed that max. deformation, which was due to max. temp. differences in the mask layers, also occurred at the end of the pulse. The anal. indicates need for exptl. study of x-ray mask distortion during exposure to short x-ray pulses (from a **laser** plasma or similar source) when the pulse amplitude reaches 10 mJ/cm2.

L18 ANSWER 43 OF 48 INSPEC COPYRIGHT 2002 IEE
AN 1991:3917299 INSPEC DN B91044640
TI Selective-area **laser**-assisted processing for **microelectronic** multi-**chip** interconnect applications.
AU Miracky, R.F. (Microelectron. & Comp. Technol. Corp., Austin, TX, USA)
SO Laser- and Particle-Beam Chemical Processes on Surfaces Symposium
Editor(s): Johnson, A.W.; Loper, G.L.; Sigmon, T.W.
Pittsburgh, PA, USA: Mater. Res. Soc, 1989. p.547-58 of xv+649 pp. 12 refs. Availability: Clarke Associates-Europe-Ltd., 13a Small Street, Bristol, UK
Conference: Boston, MA, USA, 29 Nov-2 Dec 1988
DT Conference Article
TC Practical; Experimental
CY United States
LA English
AB **Laser** direct-write processes are attractive complements to traditional methods of fabricating **microelectronic** circuitry. The author applies such processes to high-density inter-**chip** interconnection modules, such as those using copper conductors on **polyimide** dielectric layers. He begins by discussing the requirements which **laser** processes must satisfy in order to be useful in this application. An analytical model of **laser** heating is then described, which aids in understanding the thermal problem of absorption of visible-wavelength **laser** light by **polyimide**. Calculations using this model are consistent with experimental observations. Finally, he focuses on one **laser** processing technique: **laser** chemical vapor deposition. He describes a new process for **laser** chemical vapor deposition of **tungsten** on **polyimide**, which enables the formation of low resistance contacts (approximately=0.1 Omega) between the deposited **tungsten** films and pre-patterned nickel-coated copper conductors. Lines approximately 30 mu m wide and 3-4 mu m thick were deposited at a scan rate of 93 mu m/s. From four-point resistance measurements of different lengths of deposited films, the **tungsten** film resistivity is estimated to be two three times the bulk value.

L18 ANSWER 44 OF 48 HCAPLUS COPYRIGHT 2002 ACS
AN 1989:606619 HCAPLUS
DN 111:206619
TI The application of selective-area **tungsten laser** CVD to copper-on-**polyimide** multi-**chip** interconnection modules
AU Miracky, Robert F.
CS Microelectron. Comp. Technol. Corp., Austin, TX, 78727, USA
SO Tungsten Other Refract. Met. VLSI Appl. 4, Proc. Workshop (1989), Meeting Date 1988, 299-305. Editor(s): Blewer, Robert S.; McConica, Carol M. Publisher: Materials Research Society, Pittsburgh, Pa.
CODEN: 56OTAU
DT Conference
LA English

AB A new process for **laser** chem. vapor deposition of **W** on **polyimide** is described which enables the formation of low resistance contacts (.apprxeq. 0.1 .OMEGA.) between the deposited **W** films and pre-patterned Ni-coated Cu conductors. Lines .apprx.30 .mu.m wide and 3 .mu.m thick are deposited at a scan rate of 93 .mu.m/s, with little apparent damage to the underlying **polyimide**. From 4-point resistance measurements of different lengths of deposited films, the **W** film resistivity is estd. as 2-3 times the bulk value.

L18 ANSWER 45 OF 48 HCAPLUS COPYRIGHT 2002 ACS DUPLICATE 8
AN 1987:609861 HCAPLUS
DN 107:209861
TI Localized **laser** chemical processing of **tungsten** films
AU Grossman, W. M.; Karnezos, M.
CS Hewlett-Packard Lab., Palo Alto, CA, 94304, USA
SO J. Vac. Sci. Technol., B (1987), 5(4), 843-7
CODEN: JVTBD9; ISSN: 0734-211X
DT Journal
LA English
AB A focused Ar-ion **laser** beam at 514 nm was used to thermally induce localized **W** deposition from a WF6:H2 mixt. **W** lines were deposited on Si **wafers** coated with either BN or **polyimide**. Typical linewidths are 0.5-10 .mu. and the the thicknesses 0.1-1 .mu.. Linewidth correlates most strongly with **laser** power, while the thickness correlates best with the **laser** fluence delivered to the sample. A min. threshold **laser** power is needed to attain the temp. for deposition. The process is self-limiting since the deposited metal increases the surface reflectivity and thermal cond., thus increasing the threshold **laser** power. A feedback system based on measuring the reflected **laser** power during deposition was used to modulate the incident power and defeat the self-limiting nature of the process, thus allowing **W** lines to be connected. **W** deposition and etching using other gases are reported for contrast with the deposition using WF6:H2 mixts.

L18 ANSWER 46 OF 48 HCAPLUS COPYRIGHT 2002 ACS DUPLICATE 9
AN 1985:494641 HCAPLUS
DN 103:94641
TI **Laser** stimulated thermoluminescence
AU Abtahi, A.; Braunlich, P.; Kelly, P.; Gasiot, J.
CS Dep. Phys., Washington State Univ., Pullman, WA, 99164-2814, USA
SO J. Appl. Phys. (1985), 58(4), 1626-39
CODEN: JAPIAU; ISSN: 0021-8979
DT Journal
LA English
AB Exptl. and computational methods are presented for the complete characterization of the thermoluminescence response obtained from thermoluminescent phosphors upon exposure to localized Gaussian **laser** heating beams. A no. of different phosphor configurations are described as examples. These include LiF:Mg,**Ti**(TLD-100, Harshaw Chem. Corporation) in form of **chips**, which are widely used in the dosimetry of ionizing radiation, and thin-layer dosimeters prepd. either as self-supporting films or powder in a **polyimide** matrix, or on substrates of LiF single crystals or borosilicate glass. All relevant optical and thermal properties of the dosimeters can be detd.

by these methods and, based on this knowledge, the expected thermoluminescence response of a given configuration can be simulated as a function of a no. of exptl. parameters.

L18 ANSWER 47 OF 48 INSPEC COPYRIGHT 2002 IEE
AN 1987:2789248 INSPEC DN B87001610
TI Presentation of a laboratory plasma reactor: application to the analysis of defects in **integrated circuits**.
AU Araud, J.M.
SO Le Vide les Couches Minces (Nov.-Dec. 1985) no.229, suppl., p.211-15. 0 refs..
CODEN: VCMIDS ISSN: 0223-4335
Conference: 3eme Symposium International sur la Gravure Seche et le Depot Plasma en Microelectronique (3rd International Symposium on Dry Etching and Plasma Deposition in Microelectronics). Cachan, France, 26-29 Nov 1985
Sponsor(s): Union Int. Sci. & Tech. & Applications du Vide; Ministere Redeploiement Ind. & Commerce Exterieur; Minstre Recherche & Technol
DT Conference Article; Journal
TC Application; Practical
CY France
LA French
AB The importance of an effective follow-up system for monitoring the etching process for present-day semiconductor **chips** is set out. An equipment, PLASTEL, to meet the need is described; in essence it comprises a 300 **W**, 13.5 MHz RF generator, a reservoir of the reactive gases, the reactor and a RF tuner. The etching process is monitored continuously by a HeNe **laser** interferometer whose signals are processed digitally, thus giving a clear indication of end-point, easy storage of results and provision for the adjustment of several monitoring parameters. Constraints imposed by component configuration are discussed and test results are presented for **polyimide** and silicon nitride.

L18 ANSWER 48 OF 48 HCAPLUS COPYRIGHT 2002 ACS DUPLICATE 10
AN 1983:208255 HCAPLUS
DN 98:208255
TI **Laser**-formed connections using **polyimide**
AU Raffel, J. I.; Freidin, J. F.; Chapman, G. H.
CS Lincoln Lab., MIT, Lexington, MA, 02173, USA
SO Appl. Phys. Lett. (1983), 42(8), 705-6
CODEN: APPLAB; ISSN: 0003-6951
DT Journal
LA English
AB Elec. connections were formed in a new lateral link structure which uses **polyimide** in the gap between, and overlapping, 2 Al electrodes. An Ar ion **laser**, with a pulse width of 1 ms and power levels of .apprx.2 **W**, was used to locally graphitize the **polyimide**. One-k.OMEGA. connections were formed reliably in links ranging in width between 4 and 15 .mu.m and gap lengths between 2 and 5 .mu.m. This technique is the simplest yet proposed for restructuring the connections on an **integrated circuit**, after fabrication and test, to incorporate redundancy for yield improvement.

L24 ANSWER 1 OF 29 HCAPLUS COPYRIGHT 2002 ACS
AN 2002:502791 HCAPLUS
DN 137:55987
TI Self-aligned fuse structure and method with dual-thickness dielectric
IN Giust, Gary K.; Castagnetti, Ruggero; Liu, Yauh-ching; Ramesh, Subramanian
PA Lsi Logic Corporation, USA
SO U.S., 11 pp., Division of U.S. Ser. No. 118,231.
CODEN: USXXAM
DT Patent
LA English
FAN.CNT 1

PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
US 6413848	B1	20020702	US 2000-534907	20000323
PRAI US 1998-118231	A3	19980717		

AB The invention relates to a self-aligned semiconductor fuse structure in a semiconductor memory device. The fuse break point, that point at which the elec. **link** of which the fuse is part is severed by a **laser** beam, is self-aligned by the use of photolithog. patterned anti-reflective **dielec. coatings**. The self-alignment allows the size location of the break point to be less sensitive to the **laser** beam size and alignment. This has several advantages including allowing photolithog. control and effective size redn. of the **laser** spot irradiating the fuse material and surrounding structure. This permits reduced fuse pitch, increasing d. and the efficiency of use of **chip** area, and results in reduced thermal exposure, which causes less damage to **chip**. In addn., **laser** alignment is less crit. and therefore less timely, which increases throughput in fabrication.
RE.CNT 22 THERE ARE 22 CITED REFERENCES AVAILABLE FOR THIS RECORD
ALL CITATIONS AVAILABLE IN THE RE FORMAT

L24 ANSWER 2 OF 29 HCAPLUS COPYRIGHT 2002 ACS
AN 2001:851773 HCAPLUS
DN 135:379722
TI **Wafer**-scale assembly of **chip**-size packages
IN Heinen, Katherine G.; Edwards, Darvin R.; Jacobs, Elizabeth G.
PA USA
SO U.S. Pat. Appl. Publ., 17 pp.
CODEN: USXXCO
DT Patent
LA English
FAN.CNT 1

PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
US 2001044197	A1	20011122	US 1998-186973	19981105

AB A **wafer**-scale assembly app. for **integrated circuits** and a method for forming the **wafer**-scale assembly are disclosed. A semiconductor **wafer** including a plurality of circuits is provided with a plurality of metal contact pads as elec. entry and exit ports. A 1st **wafer**-scale patterned polymer film carrying solder balls for each of the contact pads on the **wafer** is positioned opposite the **wafer** and the film are aligned. The film is brought into contact with the **wafer**. Radiant energy in the near IR spectrum is applied to the backside of the

wafer, heating the **wafer** uniformly and rapidly without moving the semiconductor **wafer**. Thermal energy is transferred through the **wafer** to the surface of the **wafer** and into the solder balls, which reflow onto the contact pads, while the thermal stretching of the polymer film is mech. compensated. The uniformity of the height of the liq. solder balls is controlled either by mech. stoppers or by the precision **linear** motion of motors. After cooling, the solder balls solidify and the 1st polymer film is removed. The process is repeated for assembling sequentially a **wafer**-scale patterned interposer overlying all of the solder balls and the **wafer** and contacting each solder ball with a soldered joint, and a 2nd **wafer** -scale patterned film carrying solder balls contacting the interposer. In each process, the **wafer** is heated uniformly and rapidly and without moving it, the alignment is maintained during heating by mech. compensating for the thermal stretching of the polymer film, and the uniformity of the height of the liq. solder balls is controlled by mech. stoppers or position closed-loop **linear** actuators. The 2nd film is removed after cooling. Other embodiments are also disclosed.

L24 ANSWER 3 OF 29 HCAPLUS COPYRIGHT 2002 ACS
AN 2001:658018 HCAPLUS
DN 135:203878
TI Method of manufacturing a contact element and a multilayered **wiring** substrate, and **wafer** batch contact board by removing organics from bump holes
IN Sugihara, Osamu
PA Japan
SO U.S. Pat. Appl. Publ., 20 pp.
CODEN: USXXCO
DT Patent
LA English
FAN.CNT 1

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	US 2001019177	A1	20010906	US 2000-748022	20001227
	US 6406991	B2	20020618		
	JP 2002252258	A2	20020906	JP 2000-394250	20001226
PRAI	JP 1999-369259	A	19991227		
	JP 2000-389282	A	20001221		

AB In a method of manufg. a contact element, provision is made of a laminated body which has an **insulating film**, an elec. **conductive layer** stacked on the **insulating film**, and bump holes opened. A treatment is carried out so as to remove org. materials and the like from an interior of the bump holes and/or a surface of the **insulating film** before bumps are formed on the bump holes. The treatment may be a plasma treatment or an x-ray irradn.

L24 ANSWER 4 OF 29 HCAPLUS COPYRIGHT 2002 ACS
AN 2001:502474 HCAPLUS
DN 135:85596
TI Self-aligned fuse structure with increased density and reduced thermal exposure and method of fabrication with heat sink
IN Giust, Gary K.; Castagnetti, Ruggero; Liu, Yauh-ching; Ramesh, Subramanian
PA Lsi Logic Corporation, USA
SO U.S., 14 pp.
CODEN: USXXAM

DT Patent
LA English
FAN.CNT 1

PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
US 6259146	B1	20010710	US 1998-118232	19980717

AB Provided are a self-aligned semiconductor fuse structure, a method of making such a fuse structure, and apparatuses incorporating such a fuse structure. The fuse break point, that point at which the elec. **link** of which the fuse is part is severed by a **laser** beam, is self-aligned using photolithog. patterned dielec. and a heat sink material. The self-alignment allows the size and location of the break point to be more forgiving of the **laser** beam size and alignment. This has several advantages, including allowing photolithog. control and effective size redn. of the **laser** spot irradiating the fuse material and surrounding structure. This permits reduced fuse pitch, increasing d. and the efficiency of use of **chip** area, and results in reduced thermal exposure, which causes less damage to **chip**. In addn., **laser** alignment is less crit. and therefore less time-consuming, which increases throughput in fabrication. The present invention exploits the characteristic of most dielec. materials that they are poor conductors of thermal energy. Thermal resistance increases with the thickness of the dielec. Thus that heat is conducted more easily and thus quickly through a relatively thin portion of dielec. than it is through a relatively thick portion of dielec. In alternative embodiments, the present invention also exploits the characteristic of a dielec. material that its reflectance changes with its thickness due to optical interference effects. In such embodiments, the self-alignment of the fuse break point is further facilitated using photolithog. and anti-reflective coatings.

RE.CNT 20 THERE ARE 20 CITED REFERENCES AVAILABLE FOR THIS RECORD
ALL CITATIONS AVAILABLE IN THE RE FORMAT

L24 ANSWER 5 OF 29 HCAPLUS COPYRIGHT 2002 ACS
AN 2001:363963 HCAPLUS
DN 135:115398
TI Next generation ALIVH substrate for bare **chip** direct mounting
AU Andoh, Daizo; Sugawa, Toshio; Nakamura, Tadashi; Higashitani, Hideki; Eda, Kazuo; Tsukamoto, Masahide
CS Device Engineering Development Center, Matsushita Electric Industrial Co.,Ltd., Osaka, 571-8501, Japan
SO Proceedings - International Symposium on Advanced Packaging Materials: Processes, Properties and Interfaces, Braselton, GA, United States, Mar. 6-8, 2000 (2000), 227-232 Publisher: Institute of Electrical and Electronics Engineers, New York, N. Y.
CODEN: 69BHZK
DT Conference
LA English
AB The next generation ALIVH substrate named ALIVH-FB substrate was developed. The ALIVH-FB substrate has a structure that fine layers were formed on the surface of the conventional ALIVH substrate. The design rule of the core layer is **Line**/Space (L/S)=50/50 .mu.m, Via hole diam./Land diam. (V/L)=120/250 .mu.m and the rule of fine layer is L/S = 25/25 .mu.m, V/L = 50/150 .mu.m. Three technologies were developed (1) Thin **insulator layer** by the film material with high heat resistance, (2) fine via hole drilling process by the YAG THG **laser** and the fine interconnection technol. using the conductive

Cu paste, (3) Fabrication process of the fine layers by the transfer process. The feature is following 4 points. (1) High **wiring** d. by the Fine Via on Via structure, (2) **Film insulator** with the high heat resistance and low CTE for the high reliability of the joint between the bare **chip** and the substrate, (3) Good impedance control for the high frequency circuit, (4) Flat surface and High heat resistance for the bare **chip** mounting. The ALIVH-FB substrate is very suitable for the high pin count bare **chip** direct mounting.

RE.CNT 7 THERE ARE 7 CITED REFERENCES AVAILABLE FOR THIS RECORD
ALL CITATIONS AVAILABLE IN THE RE FORMAT

L24 ANSWER 6 OF 29 HCAPLUS COPYRIGHT 2002 ACS
AN 1999:12257 HCAPLUS
DN 130:74813
TI Manufacture of an application-specific **integrated circuit**
IN Nagura, Masahiko
PA Yamaha Corporation, Japan
SO U.S., 14 pp.
CODEN: USXXAM
DT Patent
LA English
FAN.CNT 1

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	US 5851856	A	19981222	US 1994-346672	19941130
	JP 2993339	B2	19991220	JP 1993-304441	19931203
PRAI	JP 1993-304441		19931203		

AB After an **insulating film** is deposited over metal patterns, a resist film is coated over the whole surface of the **insulating film** until the surface of the resist film becomes flat. The resist film is removed by reactive ion etching until part of the surface of the **insulating film** is exposed. Another photoresist film is coated on the surface to cover a part of the exposed areas of the **insulating film** and the resist film, exposed, and developed to form a resist mask. The area not covered with the resist mask and the resist film is selectively removed by anisotropic etching. The resist mask and the resist film are removed to obtain a window having a width equal to the width of a convex portion of the **insulating film**. A method of manufg. a semiconductor device that is capable of exposing a metal **wiring** layer with high precision is provided.

RE.CNT 28 THERE ARE 28 CITED REFERENCES AVAILABLE FOR THIS RECORD
ALL CITATIONS AVAILABLE IN THE RE FORMAT

L24 ANSWER 7 OF 29 HCAPLUS COPYRIGHT 2002 ACS
AN 1997:338903 HCAPLUS
DN 127:58733
TI **Laser** release process to obtain freestanding multilayer metal-**polyimide** circuits
AU Doany, F. E.; Narayan, C.
CS IBM Reasearch Div., Thomas J. Watson Research center, Yorktown Heights, NY, 10598, USA
SO IBM Journal of Research and Development (1997), 41(1/2), 151-157
CODEN: IBMJAE; ISSN: 0018-8646
PB International Business Machines Corp.

DT Journal
LA English
AB Some applications in **microelectronics** call for freestanding **polyimide** films with fine metallic **wiring** patterns that are thinner than com. available copper-clad **polyimide** sheets, which are typically greater than 25 .mu.m in thickness. This work describes a **laser**-assisted technique to fabricate freestanding multilayer thin-film **wiring** with **polyimide** **dielec. insulating layers** that are less than 10-.mu.m-thick. A release layer consisting of a thin polymeric film is first deposited on an optically transparent carrier, and the multilayer thin-film structure is then fabricated on this substrate, with the polymeric release layer sandwiched between the transparent carrier and the multilayer structure. Excimer **laser** light passes through the transparent carrier and ablates the polymeric layer at the transparent carrier/polymer interface, resulting in sepn. of the sacrificial carrier from the multilayer structure. The optimal release process is carried out using a 308-nm XeCl excimer **laser** operating at a fluence of about 100 mJ/cm2.

L24 ANSWER 8 OF 29 HCAPLUS COPYRIGHT 2002 ACS
AN 1997:214600 HCAPLUS
DN 126:300208
TI Investigation of ultraviolet **laser** induced **conductive layer** of silver salt filled **polyimide** films. New aspect of application of **polyimide** films
AU Kocsis, Z.; Mudra, I.; Ripka, G.
CS Department of Electronics Technology, Technical University of Budapest, H-1521, Hung.
SO NATO ASI Series, Series 3: High Technology (1996), 16(Multichip Modules with Integrated Sensors), 267-271
CODEN: NAHTF4
PB Kluwer
DT Journal
LA English
AB **Polyimides**, similar to other polymers, have found numerous applications in many areas of electronics industry. A new possible application in **microelectronics** can be their use as conductive material. The cond. of **polyimide** film surface can be changed continuously and permanently by excimer **laser** irradn. The so formed **conductive layer** contains carbon rich clusters and shows similar elec. characteristic to semiconductors. Org. silver salt was introduced into **polyimide** to promote the formation of **conductive layer**. In the irradiated layer of silver contg. polymer different conduction mechanism was found compared to that of virgin **polyimide**.

L24 ANSWER 9 OF 29 HCAPLUS COPYRIGHT 2002 ACS
AN 1997:181627 HCAPLUS
DN 126:232273
TI Semiconductor device packaging using heat spreaders and assisted deposition of **wire** bonds
IN Wills, Kendall S.; Rodriguez, Paul A.
PA Texas Instruments Inc., USA
SO U.S., 9 pp., Division of U.S. Ser. No. 98,008.
CODEN: USXXAM
DT Patent

LA English
FAN.CNT 1

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	US 5605863	A	19970225	US 1995-472103	19950607
PRAI	US 1990-575744		19900831		
	US 1992-817972		19920106		
	US 1993-98008		19930727		

AB A process for manufg. device or **die** packaging uses **laser** -deposited leads, with a filler to bridge the gap between the **die** and the lead frame. The filler may be oxide, **polyamide**, a combination of **oxide layers** and **polyamide** layers, plastic, or a plastic which has plastic-coated beads of metal. The **die** and lead frame are placed on a heat spreader. Leads are formed over the filler material from bond pads on the lead frame to bond pads on the **die**. Various protective materials are placed over the **die** to protect it from the package. Over the protective material is another heat spreader or other device that is required to make the **die** function better. Finally, the structure is encapsulated in a package of nonconductive material.

L24 ANSWER 10 OF 29 HCAPLUS COPYRIGHT 2002 ACS
AN 1996:650937 HCAPLUS
DN 125:289997
TI Time reduction of MCM-D prototype realization by process control and modeling.
AU Fremont, H.; Ahrens, C.; Christophe, E. Saint; Enockl, B.; Fathi, M.; N'kaoua, G.; Pellet, C.; Ferretti, R.; Danto, Y.
CS IXL - URA 846, Universite Bordeaux I, Talence, 33405, Fr.
SO Proceedings of SPIE-The International Society for Optical Engineering (1996), 2874(Microelectronic Manufacturing Yield, Reliability, and Failure Analysis II), 138-149
CODEN: PSISDG; ISSN: 0277-786X
PB SPIE-The International Society for Optical Engineering
DT Journal
LA English
AB The evolution of advanced packaging techniques like Multi **Chip** Modules makes the realization of prototypes necessary. This can be a long and costly operation. Therefore the authors developed methods permitting time gains to be made in two of the steps of this operation. To avoid the use of phys. masks the authors have experimented a **laser** beam set for direct writing of metal and **insulating layers** in **microcircuits**. To shorten preliminary tests, the authors propose a theor. model of the interaction between the **laser** beam and the photoresist. It permits one to predict the **line** widths etched in the photoresist and thus avoids the need of long calibration processes. Elec. test **lines** of various widths were used as a validation tool. The precision obtained is better than 5%. **Polyimides** (PI) meet most of the requirements for dielec. materials. As the curing process is crucial for the properties of the final PI film, thermal treatment was subjected to optimization leading however to process times up to >4 h. The authors developed an interferometric control system in combination with a hot plate, to provide an automated and optimized curing process. Total curing time is reduced to 1-2 h. Characterization and FTIR measurements were done for conventional and interferometrically controlled curing samples before and after aging in wet atm. Controlled samples are more cryst., show

comparable elec. and reliability properties, and seem less stressed.

L24 ANSWER 11 OF 29 HCAPLUS COPYRIGHT 2002 ACS
AN 1995:634900 HCAPLUS
DN 123:89949
TI Metal capping of MCM thin film features using a **laser**
AU Patel, R. S.; Wassick, T. A.; Ralston, C. Y.
CS IBM Microelectronics Division, Hopewell Junction, NY, 12533-6531, USA
SO Proceedings - Electronic Components & Technology Conference (1994), 44th, 353-8
CODEN: PETCES
PB Institute of Electrical and Electronics Engineers
DT Journal
LA English
AB A **laser** process to provide a thin barrier or capping metal, over the copper features of a multichip module thin film (MCM-D) structure is described. Capping of copper features is required to avoid copper corrosion and diffusion into overlaying **dielec. layers** of thin film structure. Furthermore, in a multilevel thin film structure, certain barrier metals provide improved adhesion for the subsequent **dielec. layer**. Expts. with XeCl and Nd-Yag **lasers** were performed to det. the best **laser** source for Cr capping of a copper/polymer/ceramic material set. The **laser** capping process is more robust and quicker than conventional photolithog. or electroless plating capping processes, while eliminating the wet chem. operations. Also, the **laser** capping process eliminates the undercapping and variable capping metal thickness problems assocd. with photolithog. and/or electroless plating techniques. The results of capping metal features on bare glass ceramic and polymer surfaces are described.

L24 ANSWER 12 OF 29 HCAPLUS COPYRIGHT 2002 ACS
AN 1995:377353 HCAPLUS
DN 122:303870
TI M4CMS (thin film Multi-MMic Multi-**IC** Modules) for microwave applications
AU Feurer, Ernst; Oppermann, Martin; Holl, Bruno
CS Deutsche Aerospace (Dasa), Ulm, 89077, Germany
SO Proceedings of SPIE-The International Society for Optical Engineering (1994), 2369(27th International Symposium on Microelectronics, 1994), 49-53
CODEN: PSISDG; ISSN: 0277-786X
DT Journal
LA English
AB Microwave Transmit/Receive (T/R) modules for modern radar applications were realized with multilayer integration technol. The M4-multilayer is designed and fabricated in thin film technol. on Al2O3 ceramic substrates and offers a high order of complexity for radio frequency (rf) circuits up to 20 GHz. Single-face and double-face structured and populated MCM substrates are presented. Microstrip **lines** with integrated thin film resistors in combination with the **dielec.** spaced ground **layer** on the opposite side define the radiofrequency layer on top of the substrate. The multilayer logic control unit consists of three metal layers (ground-, x-, y-conductor plane), each sepd. by patterned polymeric dielecs. (**polyimide**, benzocyclobutene). This paper describes the necessary technol. steps for high performance in thin film multilayer technol. in regard to cost driven microwave applications.

L24 ANSWER 13 OF 29 HCAPLUS COPYRIGHT 2002 ACS
AN 1993:223471 HCAPLUS
DN 118:223471
TI Fabrication of via-holes in multi-**chip** module using third harmonic generation of Nd:YAG **laser**
AU Gofuku, Eishi; Ohnawa, Toshio; Takada, Mitsuyuki; Matsukawa, Fumio; Nunoshita, Masahiro
CS Mater. and Electron. Devices Lab., Mitsubishi Electr. Corp., 1-1 Tsukaguchi Honmachi 8-chome, Amagasaki, Hyogo, 661, Japan
SO Appl. Surf. Sci. (1993), 64(4), 353-60
CODEN: ASUSEE; ISSN: 0169-4332
DT Journal
LA English
AB In the fabrication of high-speed digital **integrated circuits** using **polyimide films** as **insulators**, esp. multi-**chip** modules (MCMs), via-holes of 20 .mu.m depth have to be realized for the characteristic impedance along the signal **line**. When a logical scale in a near-feature engineering work station (EWS) is considered, the no. of via-holes does not exceed 600 in one circuit. In this work, the authors propose the possibility of applying a third harmonic generation (THG) of a Q-switched Nd:YAG **laser** to drill high-aspect-ratio via-holes in such a thick **polyimide** film. The drilled holes as well as the excimer **laser** exhibit excellent configurations. The THG **laser** system is applicable to the fabrication process of the MCM.

L24 ANSWER 14 OF 29 HCAPLUS COPYRIGHT 2002 ACS
AN 1993:181306 HCAPLUS
DN 118:181306
TI **Laser** methods for circuit repair on **integrated circuits** and substrates
IN Donelon, John J.; Dovle, James P.; Hurst, Jerry E., Jr.; Rossnagel, Stephen M.
PA International Business Machines Corp., USA
SO U.S., 11 pp. Cont.-in-part of U.S. Ser. No. 233,487.
CODEN: USXXAM
DT Patent
LA English
FAN.CNT 1

PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI US 5171709	A	19921215	US 1991-770838	19911004

AB A method, of forming an elec. **conductive film** layer in the surface of a substrate, includes (a) irradiating the substrate surface with an ion beam for a 1st period of time sufficient to form a carbonaceous surface region thereon; (b) allowing the substrate to cool for a 2nd period of time between 15 s and 5 min.; and (c) repeating steps (a) and (b) until the sheet resistance of the carbonaceous surface region reaches a predetd. value.

L24 ANSWER 15 OF 29 HCAPLUS COPYRIGHT 2002 ACS
AN 1991:644970 HCAPLUS
DN 115:244970
TI Multichip-module interconnections by **laser** direct writing
AU Mueller, Heinrich G.; Paredes, Alvaro; Buschick, Klaus; Reichl, Herbert
CS Tech. Univ. Berlin, Berlin, D-1000/65, Fed. Rep. Ger.

SO Mater. Res. Soc. Symp. Proc. (1991), 203(Electron. Packag. Mater. Sci. 5), 369-74
CODEN: MRSPDH; ISSN: 0272-9172
DT Journal
LA English
AB A very flexible maskless technique is described for thin-film hybrid formation. **Dielec. layers** of **polyimide** are formed by spin-on techniques and are then **laser** structured for via hole formation. Interconnections of the embedded **chips** are generated by **laser** direct writing of thin Cu **lines** from Cu formate, followed by chem. Cu deposition. Chem. pretreatments of the Al contact pads allow for reasonable **chip** contacting with these methods.

L24 ANSWER 16 OF 29 HCAPLUS COPYRIGHT 2002 ACS
AN 1991:93237 HCAPLUS
DN 114:93237
TI Isolated microstrip transmission **line** and its manufacture
PA University of California, Oakland, USA
SO Jpn. Kokai Tokkyo Koho, 9 pp.
CODEN: JKXXAF
DT Patent
LA Japanese
FAN.CNT 1

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	JP 02140931	A2	19900530	JP 1989-187228	19890719
	US 5017509	A	19910521	US 1990-555814	19900718
PRAI	US 1988-221395		19880719		

AB A method for manufg. a transmission **line** on an **integrated circuit** structure having a metal grounding surface involves the following steps: (1) forming a **dielec. layer** on the grounding surface; (2) forming a microstrip transmission **line**(s) on the **dielecs. layer**; (3) removing the **dielec. layer** from outside of the **line**(s) to form a post for the **line**(s). Optionally, in the 1st step, the dielecs. may be SiO2 or **polyimide** having about 10 .mu.m thickness, in the 2nd step, addnl. **dielec. layer** may be formed and the transmission **line** may be formed on the addnl. layer and/or in the 3rd step, the **dielec. layer** may be removed by reactive ion etch to the ground surface by using a C coating on the microstrip **line** as a mask. The 2nd step may involve forming a metal layer and a mask layer(s) (SiO2 and amorphous Si) on the **dielec. layer**, patterning the mask layer(s) to expose the metal layer by **laser** etching the amorphous Si layer and wet chem. etching, plasma etching, or reactive ion etching) the SiO2 layer, and coating, such as electroplating and electroless plating, removing the mask layer and the extra metal layer by ion, miling, electropolishing, plasma etching, or wet chem. etching. A microstrip transmission **line** formed on an **integrated circuit wafer**, which has a large impedance characteristic, small crosstalk, high transmission speed, and a small **wafer** stress, is obtained.

L24 ANSWER 17 OF 29 HCAPLUS COPYRIGHT 2002 ACS
AN 1988:603318 HCAPLUS
DN 109:203318

TI Method for producing via holes in polymer dielectrics
IN Loughran, James A.; McMullen, James G.; Yerman, Alexander J.
PA General Electric Co., USA
SO U.S., 7 pp.
CODEN: USXXAM
DT Patent
LA English
FAN.CNT 1

PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
US 4764485	A	19880816	US 1987-617	19870105

AB A method for producing a hole in a polymer film includes the steps of depositing a **conductive layer** onto the polymer film and irradiating a spot on the layer with a burst of focused **laser** energy at a level sufficient to form an opening in the film and, subsequently, plasma etching the film so as to form a hole of desired depth in the polymer film underlying the opening in the **conductive layer**. This method is particularly applicable to the formation of multichip **integrated circuit** packages in which a no. of **chips** formed in a semiconductor **wafer** are coated with a polymer film covering the **chips** and the substrates. The holes are provided to interconnect selected **chip** contact pads via a deposited **conductive layer** which overlies the film and fills the holes.

L24 ANSWER 18 OF 29 INSPEC COPYRIGHT 2002 IEE
AN 1999:6161023 INSPEC DN B1999-03-2210D-074
TI **Laser** excising of flexible circuits.
AU Gu, B.; Moffat, S.; Young, B. (Lumonics Inc., Kanata, Ont., Canada)
SO IPC Fourth Annual National Conference on Flexible Circuits: Meeting the Challenge of the Next Generation of Packaging
Northbrook, IL, USA: Inst. Interconnecting & Packaging Electron. Circuits, 1998. p.57-64 vol.1 of 2 vol. (138+132+23 Addendum) pp. 3 refs.
Conference: San Jose, CA, USA, 18-19 March 1998
ISBN: 1-580985-23-8
DT Conference Article
TC Application; Practical; Experimental
CY United States
LA English
AB Flexible printed circuit (FPC) manufacturers are challenged by the increases in interconnect **line** and contact pad density required to match the continual increase in **IC** density. As conductor pattern density increases, both circuit dimensions and their tolerances decrease. Many conventional mechanical and chemical processing techniques become either technically or financially impractical. **Laser** processing is one of the advanced techniques that can be adopted in FPC fabrication. In this paper, we present the results of a systematic study of **laser** routing of circuits. **Laser** routing requires no hard tooling and therefore offers greater flexibility because the design can be directly input into the **laser**-machining controller. This allows short-term prototype circuits to be excised quickly and cost effectively. CO2 **lasers** are the most widely used in circuit excision. We have conducted a series of experiments aimed at cutting process characterization for the most commonly used dielectric materials (**polyimide**, epoxy glass, polyester) of varying thickness using different **lasers** (TEA CO2, CW RF-excited CO2). The influence of the **laser** pulse width, **laser** average

power and **laser** beam spot size on cutting performance have been assessed in terms of edge quality, cut width and optimum cutting speed. Different beam delivery systems for different types of **lasers** are also discussed.

L24 ANSWER 19 OF 29 INSPEC COPYRIGHT 2002 IEE
AN 1998:6057397 INSPEC DN B9812-2250-001
TI Application of BPDA/PDA **polyimide** films in multi-**chip** modules (MCM).
AU Ishizuki, Y.; Yokouchi, K.; Yoneda, Y. (Fujitsu Labs. Ltd., Atsugi, Japan)
SO Journal of Photopolymer Science and Technology (1998) vol.11, no.2, p.253-6. 6 refs.
Published by: Tech. Assoc. Photopolymers
CODEN: JSTEEW ISSN: 0914-9244
SICI: 0914-9244(1998)11:2L.253:ABPF;1-J
DT Journal
TC Experimental
CY Japan
LA English
AB **Polyimides** are widely used as dielectrics in high density multi-**chip** module (MCM) **wiring** systems in order to adjust the thermal expansion between LSI **chips** and substrates. In these MCMs, Copper is commonly used for vias which interconnects different layers. In these structures, there are some drawbacks which adversely affect the multi-layer **wiring** system. Among them, a major problem is that in order to get a high **wiring** density, a large number of vias with a very small via diameter have to be created. However, if there are large number of vias, due to the Z-directional thermal expansion mismatch of Cu and the dielectric, stress concentrated around vias leading to fracture and crack formation in the dielectric. Therefore, in this paper, in order to find a promising dielectric material, to the utilized in MCMs, the Z-directional coefficient of thermal expansion (CTE) of **polyimide** films prepared with different processing conditions was investigated. The Z-directional CTE of the films was measured by the **laser** interferometric technique.

L24 ANSWER 20 OF 29 INSPEC COPYRIGHT 2002 IEE
AN 1998:5793644 INSPEC DN B9802-2210D-023
TI PERL-an FR4 based micro via technology.
AU Olbrich, W. (Hewlett-Packard GmbH, Boblingen, Germany)
SO Recent Progress in Printed Circuit Board Technology
Berlin, Germany: Fraunhofer-Inst. IZM, 1997. p.11 pp. of 176 pp. 3 refs.
Conference: Berlin, Germany, 27-29 Jan 1997
DT Conference Article
TC Application; Practical
CY Germany, Federal Republic of
LA English
AB PERL (plasma etched redistribution layer) technology allows PCB manufacture in FR4 or high Tg FR4 material, including microvias. The technology was developed from the **polyimide** based DYCOstrate process. PERL multilayer board production is very similar to that of conventional PCBs. A new resin coated copper foil material is used to form the outer Cu **layers** and **dielectric layers**.
Conventional FR4 or high Tg FR4 cores are used as inner layers. A via mask is generated by photoprocessing following multilayer lamination. The microvias are plasma etched in a newly developed plasma drilling machine. All other processes are standard PCB processes. The advantages of the

technology are its compatibility with conventional PCBs in terms of materials, assembly, electrical properties and reliability, and the capability for very high density **wiring**, which may be used to reduce board size and layer count, to introduce greater PCB functionality and to utilize new components such as high I/O count **chip** scale packages. The typical microvia pad size is 12 mil. Striplines with controlled impedances of 50 Omega are possible in PERL layers. Manufacturing cost is comparable to conventional boards, as there are few process sequence changes. Many constructions include buried vias or sequentially laminated cores, giving greater design freedom. Typical PERL products are MCMs, computer boards, computer peripheral and telecom boards. This paper describes the manufacturing sequence, materials and reliability data along with typical constructions, and assesses the future potential of this technology, including **laser** drilling technology and the amount of materials.

L24 ANSWER 21 OF 29 INSPEC COPYRIGHT 2002 IEE
AN 1997:5611680 INSPEC DN B9708-2220E-001
TI **Laser** release process to obtain freestanding multilayer metal-**polyimide** circuits.
AU Doany, F.E.; Narayan, C. (IBM Thomas J. Watson Res. Center, Yorktown Heights, NY, USA)
SO IBM Journal of Research and Development (Jan.-March 1997) vol.41, no.1-2, p.151-7. 8 refs.
Published by: IBM
Price: CCCC 0018-8646/97/$5.00
CODEN: IBMJAE ISSN: 0018-8646
SICI: 0018-8646(199701/03)41:1/2L.151:LRPO;1-Y
DT Journal
TC Experimental
CY United States
LA English
AB Some applications in **microelectronics** call for freestanding **polyimide** films with fine metallic **wiring** patterns that are thinner than commercially available copper-clad **polyimide** sheets, which are typically greater than 25 mu m in thickness. This work describes a **laser**-assisted technique to fabricate freestanding multilayer thin-film **wiring** with **polyimide** **dielectric insulating layers** that are less than 10 mu m thick. A release layer consisting of a thin polymeric film is first deposited on an optically transparent carrier and the multilayer thin-film structure is then fabricated on this substrate, with the polymeric release layer sandwiched between the transparent carrier and the multilayer structure. Excimer **laser** light passes through the transparent carrier and ablates the polymeric layer at the transparent carrier/polymer interface, resulting in separation of the sacrificial carrier from the multilayer structure. The optimal release process is carried out using a 308-nm XeCl excimer **laser** operating at a fluence of about 100 mJ/cm2.

L24 ANSWER 22 OF 29 INSPEC COPYRIGHT 2002 IEE
AN 1997:5560816 INSPEC DN B9706-2250-001; C9706-3350E-002
TI Time reduction of MCM-D prototype realization by process control and modeling.
AU Fremont, H.; Ahrens, C.; Saint Christophe, E.; Enockl, B.; Fathi, M.; N'kaoua, G.; Pellet, C. (Bordeaux I Univ., Talence, France); Ferretti, R.; Danto, Y.

SO Proceedings of the SPIE - The International Society for Optical Engineering (1996) vol.2874, p.138-49. 5 refs.
Published by: SPIE-Int. Soc. Opt. Eng
Price: CCCC 0 8194 2272 X/96/$6.00
CODEN: PSISDG ISSN: 0277-786X
SICI: 0277-786X(1996)2874L.138:TRPR;1-D
Conference: Microelectronic Manufacturing Yield, Reliability, and Failure Analysis II. Austin, TX, USA, 16-17 Oct 1996
Sponsor(s): SPIE
DT Conference Article; Journal
TC Practical; Theoretical; Experimental
CY United States
LA English
AB The evolution of advanced packaging techniques like multichip modules makes the realization of prototypes necessary. This can be a long and costly operation. We therefore developed methods permitting time gains to be made in two of the steps of this operation. In order to avoid the use of physical masks, we have experimented with a **laser** beam set for direct writing of metal and **insulating layers** in **microcircuits**. To shorten preliminary tests, we propose a theoretical model of the interaction between the **laser** beam and the photoresist. It permits us to predict the **line** widths etched in the photoresist and thus avoids the need of long calibration processes. Electrical test **lines** of various widths have been used as a validation tool. The precision obtained is better than 5%. **Polyimides** (PI) meet most of the requirements for dielectric materials. As the curing process is crucial for the properties of the final PI film, thermal treatment was subject to optimization, leading however to process times of more than 4 hours. We developed an interferometric control system in combination with a hot plate in order to provide an automated and optimized curing process. Total curing time is reduced to 1-2 hours. Characterization and FTIR measurements were done for conventional and interferometrically controlled curing samples before and after ageing in a wet atmosphere; the controlled samples were more crystalline, showed comparable electrical and reliability properties, and seem less stressed than the conventional samples.

L24 ANSWER 23 OF 29 INSPEC COPYRIGHT 2002 IEE
AN 1997:5507743 INSPEC DN B9704-2250-007
TI Investigation of ultraviolet **laser** induced **conductive layer** of silver salt filled **polyimide** films.
AU Kocsis, Z. (Dept. of Electron. Technol., Budapest Tech. Univ., Hungary); Mudra, I.; Ripka, G.
SO Multichip Modules with Integrated Sensors. Proceedings of the NATO Advanced Res Workshop
Editor(s): Jones, K.W.; Harsanyi, G.
Dordrecht, Netherlands: Kluwer Academic Publishers, 1996. p.267-71 of ix+324 pp. 16 refs.
Conference: Budapest, Hungary, 18-20 May 1995
ISBN: 0-7923-4194-5
DT Conference Article
TC Application; Practical; Experimental
CY Netherlands
LA English
AB **Polyimides**, similar to other polymers, have found numerous applications in many areas of the electronics industry. A new possible application in **microelectronics** is their use as a conductive

material. The conductivity of the **polyimide** film surface can be changed continuously and permanently by excimer **laser** irradiation. The thus formed **conductive layer** contains carbon rich clusters and shows similar electrical characteristics to semiconductors. Organic silver salt was introduced into the **polyimide** to promote formation of the **conductive layer**. In the irradiated layer of silver-containing polymer, a different conduction mechanism was found compared to that of virgin **polyimide**.

L24 ANSWER 24 OF 29 INSPEC COPYRIGHT 2002 IEE
AN 1995:5064805 INSPEC DN B9511-2575-011
TI Development of coil winding process for radial gap type electromagnetic micro-rotating machine.
AU Ota, H. (Central Res. Lab., Mitsubishi Electr. Corp., Tokyo, Japan); Oda, T.; Kobayashi, M.
SO Proceedings. IEEE Micro Electro Mechanical Systems 1995 (Cat. No.95CH35754)
New York, NY, USA: IEEE, 1995. p.197-202 of 418 pp. 6 refs.
Conference: Amsterdam, Netherlands, 29 Jan-2 Feb 1995
Sponsor(s): IEEE Robotics & Autom. Soc.; ASME Dynamic Syst. & Control Div
ISBN: 0-7803-2503-6
DT Conference Article
TC Practical
CY United States
LA English
AB This paper presents a manufacturing process for forming the coil winding on a cylindrical core to make a stator for a micro-generator. A cylindrical stator of 1 mm in diameter and 0.5 mm in length was fabricated. This stator consists of a cylindrical core made of permalloy and six coils of copper **wire** with a cross section of 7 mu m*15 mu m which were wound 20 turns per coil and with 2 mu m thick **polyimide insulation layers**. The stator was fabricated by securing the coil onto the core **die**, and electroplating the remaining area with permalloy. A micro-generator 1.2 mm in diameter was fabricated incorporating this stator, and the voltage induced by the generator was measured. Examination revealed that the newly developed process is applicable to the manufacture of electromagnetic micro-devices.

L24 ANSWER 25 OF 29 INSPEC COPYRIGHT 2002 IEE
AN 1993:4401209 INSPEC DN B9306-2220J-009
TI Fabrication of via-holes in multi-**chip** module using third harmonic generation of Nd:YAG **laser**.
AU Gofuku, E.; Ohnawa, T.; Takada, M.; Matsukawa, F.; Nunoshita, M. (Mater. & Electron Devices Labs., Mitsubishi Electric Corp., Hyogo, Japan)
SO Applied Surface Science (April 1993) vol.64, no.4, p.353-60. 13 refs.
Price: CCCC 0169-4332/93/$06.00
CODEN: ASUSEE ISSN: 0169-4332
DT Journal
TC Practical; Experimental
CY Netherlands
LA English
AB In the fabrication of high-speed digital **integrated circuits** using **polyimide films** as **insulators**, especially multi-**chip** modules (MCMs), via-holes of 20 mu m depth have to be realized for the characteristic

impedance along the signal **line**. When a logical scale in a near-feature engineering work station (EWS) is considered, the number of via-holes does not exceed 600 in one circuit. In this work, the authors propose the possibility of applying a third harmonic generation (THG) of a Q-switched Nd:YAG **laser** to drill high-aspect-ratio via-holes in such a thick **polyimide** film. The drilled holes as well as the excimer **laser** exhibit excellent configurations. The THG **laser** system is applicable to the fabrication process of the MCM.

L24 ANSWER 26 OF 29 INSPEC COPYRIGHT 2002 IEE
AN 1991:4000768 INSPEC DN B91069476
TI Multi-**chip**-module interconnections by **laser** direct writing.
AU Muller, H.G.; Paredes, A.; Buschick, K.; Reichl, H. (Tech. Univ., Berlin, Germany)
SO Electronic Packaging Materials Science V. Symposium
Editor(s): Lillie, E.D.; Ho, P.S.; Jaccodine, R.; Jackson, K.
Pittsburgh, PA, USA: Mater. Res. Soc, 1991. p.369-74 of xiii+455 pp. 8 refs.
Conference: Boston, MA, USA, 26-29 Nov 1990
Sponsor(s): Mater. Res. Soc
DT Conference Article
TC Experimental
CY United States
LA English
AB A very flexible maskless technique for thin film hybrid formation has been developed. Layouts are transferred directly from work stations to **laser** controls. Openings in ceramic substrates are achieved through **laser** cutting, and **chips** are embedded to give a common **chip**-to-substrate surface, flat to within 2 mu m. **Dielectric layers** of **polyimide** are formed by spin on techniques and are then **laser** structured for via hole formation. Interconnections of the embedded **chips** are generated by **laser** direct writing of thin copper **lines** from copper formate, followed by chemical copper deposition. Chemical pretreatments of the aluminum contact pads allow for reasonable **chip** contacting with these methods. Electrical measurements on the DC **line** conductivity and the high frequency behaviour of these interconnections have also been performed.

L24 ANSWER 27 OF 29 INSPEC COPYRIGHT 2002 IEE
AN 1991:3897395 INSPEC DN B91038124
TI Engineering change (EC) technology for thin film metallurgy on **polyimide** films.
AU Ray, S.K.; Seshan, K.; Interrante, M. (IBM, East Fishkill, NY, USA)
SO 1990 Proceedings. 40th Electronic Components and Technology Conference (Cat. No.90CH2893-6)
New York, NY, USA: IEEE, 1990. p.395-400 vol.1 of 2 vol. xvi+1125 pp. 14 refs.
Conference: Las Vegas, NV, USA, 20-23 May 1990
Sponsor(s): IEEE; Electron. Ind. Assoc
Price: CCCC 0569-5503/90/0000-0395$01.00
DT Conference Article
TC New Development; Practical; Experimental
CY United States
LA English
AB Engineering change in multichip modules such as the IBM Thermal Conduction

Module (TCM) requires making new nets on the top surface of the module. This is done either to repair opens or shorts in the internal nets or to correct design errors. Since the trend in multichip packaging in the high end is towards thin-film **wiring** with **polyimide** as the dielectric, **wire**-bond and **laser** delete processes compatible with thin-film metallurgy on **polyimide** films are required to carry out engineering change. The authors describe the results of a technology-development effort to optimize these processes on a metal/ **polyimide** thin-film structure.

L24 ANSWER 28 OF 29 INSPEC COPYRIGHT 2002 IEE
AN 1988:3140701 INSPEC DN B88033359
TI Energy beam induced conductivity in **polyimide** films: application to micropatterning.
AU Davenas, J.; Xu, S.L.; Boiteux, G.; Nouvel, O. (Univ. Claude Bernard, Villeurbanne, France)
SO 2nd International Conference on Passive Components: Materials, Technologies, Processing
Paris, France: Comite Colloque Int. Composants Passifs, Nov. 1987. p.66-71 of xxii+417 pp. 17 refs.
Conference: Paris, France, 18-20 Nov 1987
Sponsor(s): CNET; CNRS; Eur. Electron. Component, Manuf. Assoc.; et al
DT Conference Article
TC Application; Experimental
CY France
LA French
AB There are two main routes for producing polymers exhibiting conductive properties. The synthesis of inherent conducting polymers and the energy beam modification of intrinsic insulators in order to produce conducting layers. Energy beams allow the definition of fine features in complex structures. The formation of 'conductive **polyimide**' using **lasers** or ion beams provide a method for producing conducting patterns in polymers exhibiting the required stability and processability conditions for their use in **microelectronics**. Ion beam conditions have been studied in order to form **conductive layers** of 1000 AA thick in kapton, with conductivities ranging from 100 to 1000 S/cm.

L24 ANSWER 29 OF 29 INSPEC COPYRIGHT 2002 IEE
AN 1984:2255872 INSPEC DN B84030218
TI Pulsed **laser** generation of vias in thin **polyimide** layers.
AU Ray, S.K. (IBM Corp., Armonk, NY, USA)
SO IBM Technical Disclosure Bulletin (Dec. 1983) vol.26, no.7B, p.3586-7. 0 refs.
CODEN: IBMTAA ISSN: 0018-8689
DT Journal
TC Practical; Experimental
CY United States
LA English
AB A method is disclosed for forming vias through a **polyimide insulating layer** between **wiring** planes using a pulsed **laser**.